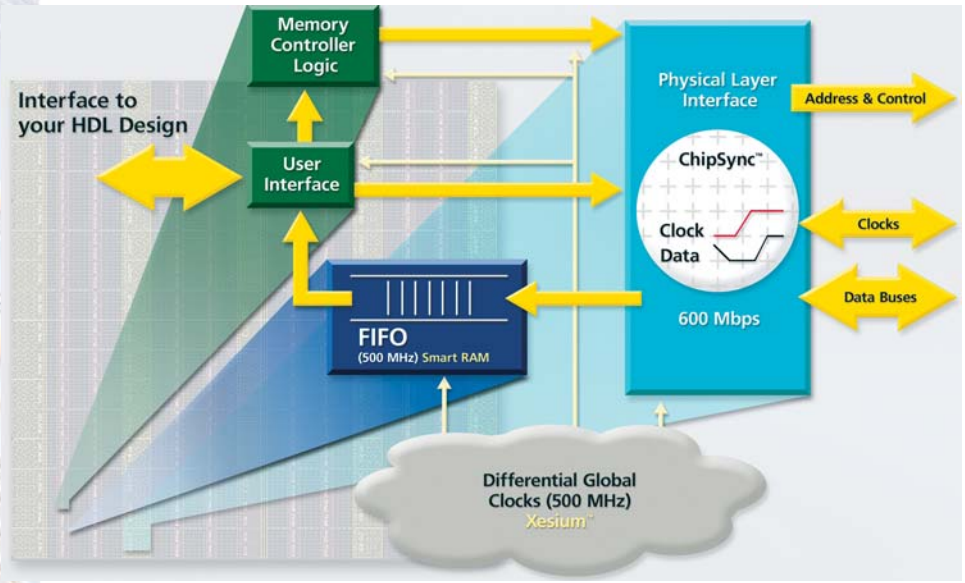
Virtex-4™ Memory Interfaces

Hardware-Proven Solutions

Building interfaces to high-performance memory devices presents challenges such as high-speed synchronous data capturing, along with implementing complex physical-layer interfaces and control logic.

Virtex-4™ FPGAs solve these challenges with advanced silicon capabilities, including ChipSync™ source-synchronous technology, Xesium™ clocking, and Smart RAM. These features deliver the performance you need, while using minimal logic fabric resources.

To shrink design time, Xilinx provides expert guidance in the form of free, hardware-verified reference designs, application notes, user-friendly tools, and advanced development systems. This combination of unique silicon capabilities and comprehensive support enables you to build and verify robust memory interfaces quickly and easily.



High-Performance, Cost-Effective Solutions to Simplify Memory Interface Design

Optimize Your Design with Unique Built-in Silicon Features

- Revolutionary ChipSync technology provides 80 ps resolution for clock-to-data alignment, ensuring reliable data capture
- 500 MHz Xesium differential global clocks minimize skew and jitter, providing increased design margins
- 500 MHz Smart RAM blocks have built-in FIFO functionality, minimizing the design size
- Column-based I/O eliminates memory interface placement restrictions, alleviating board congestion

Finish Faster Using Proven Memory Interface Designs

- Comprehensive suite of free hardware-verified reference designs for high-speed memory interfaces (DDR2, DDR, QDR II, RLDRAM II, FCRAM II)
- Choose between fully synthesizable VHDL and Verilog reference designs

Customize with Ease Using Hardware Development Board

- Implement modifications with user-friendly tools
- Verify customizations with an advanced development board created specifically for memory interface design

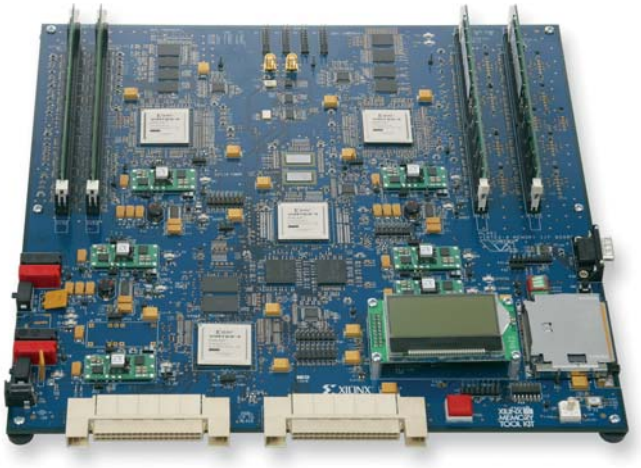
XILINX®

Proven Memory Interface Solutions

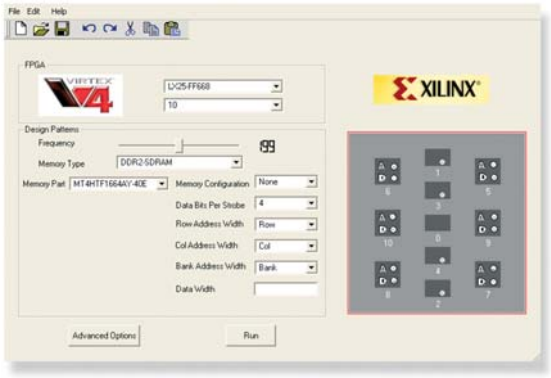
Xilinx offers a complete suite of resources to support you in building and testing memory interfaces:

- **Advanced Memory Development System –** Develop and verify your design in hardware
- **Free Reference Designs and Detailed Application Notes**
- **Memory Interface Generator –** Customize your design with a simple menu-based tool
- **ChipScope™ Pro –** Debug, analyze and verify your design in real-time
- **Memory Corner Web Resources**
- **Education Services –** Increase your skill set and reduce your time-to-knowledge

Advanced Memory Development System



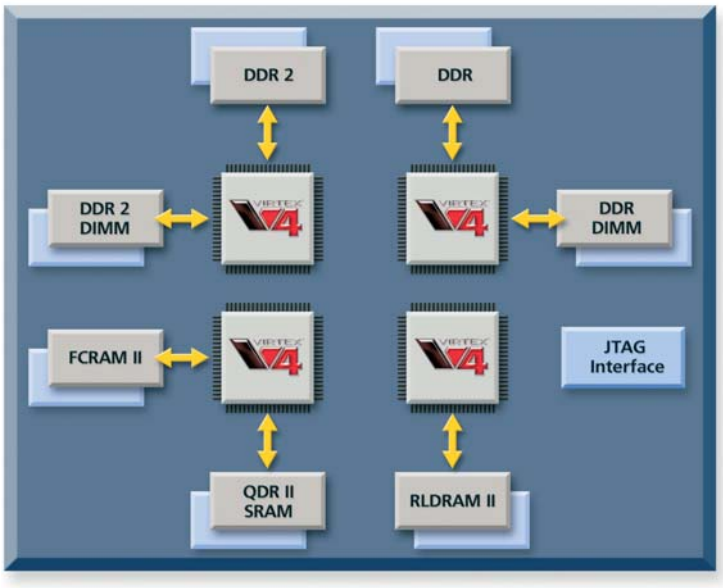
Memory Interface Generator



Memory System Features

Parameter	DDR2 SDRAM	DDR SDRAM	QDR II	RLDRAM II	FCRAM II
Data Rate	534 Mbps	400 Mbps	1.2 Gbps	600 Mbps	600 Mbps
CLK Rate	267 MHz	200 MHz	300 MHz	300 MHz	300 MHz
Data Width	144 bit (DIMM) 28 bit	144 bit (DIMM) 28 bit	(72+72) bit	36 bit	36 bit
I/O Standard	SSTL 18	SSTL 2	HSTL	HSTL	SSTL 18

ML461 Advanced Memory Development System Block Diagram



Take the Next Step

For the latest information or to find out more about our complete Virtex-4 FPGA memory solutions, visit **www.xilinx.com/virtex4**

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