ECE 4170: Introduction to HDL with Applications to Digital System Design

School of Electrical and Computer Engineering
Georgia Institute of Technology
Spring 2007 Semester
Instructor: Prof. Sudhakar Yalamanchili

Template for Completed & Tested Module Report

Submission Date: April 17th 2007, 9pm

Have Questions?: Please e-mail or meet TA

Your report for tested, completed modules needs to have the following sections.

1. Block Diagram of Computation Core

This diagram should show the presence and interconnection of all custom VHDL modules in your computation core. Make bit widths and directionality of buses clear, and indicate which modules have been completed and tested. Approximately 25-30% of your functional design should be completed and tested by this point. Include a listing following the diagram that states the functions performed by each block.

2. Completed Modules

Provide the entity and architecture for each completed module, and include a waveform of each module's simulation (the waveform need not show an exhaustive simulation, but can be zoomed in to clearly show operation for three or four situations).

3. Design Changes & Problems

Briefly describe any design changes you were forced to make after beginning to develop your computation components. In addition, outline any difficulties you faced in getting major components to simulate or synthesize properly. It can be very helpful to try to synthesize these smaller components as you develop them; it will give you rough estimates of timing and area consumption to consider while working on the rest of your design, and it will notify you of synthesis problems before your design becomes unwieldy. Please check the Xilinx Implementation Tutorial on the class website for help in this regard.

Submit a zip file with the above elements to Professor Yalamanchili with a copy to the TA by 9pm, Tuesday April 17th.