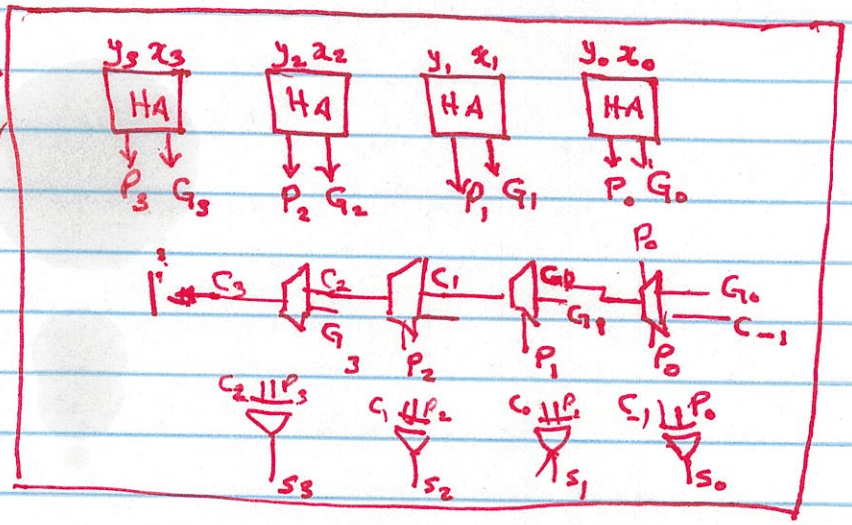
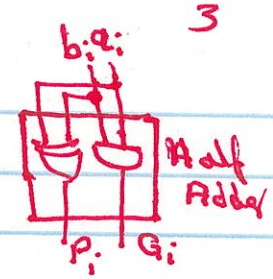
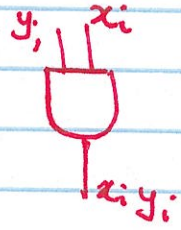
COEN 6501 Oct. 2019

Q1 4-bit Manchester Carry Adder







$x_3\ x_2\ x_1\ x_0$

$y_3\ y_2\ y_1\ y_0$

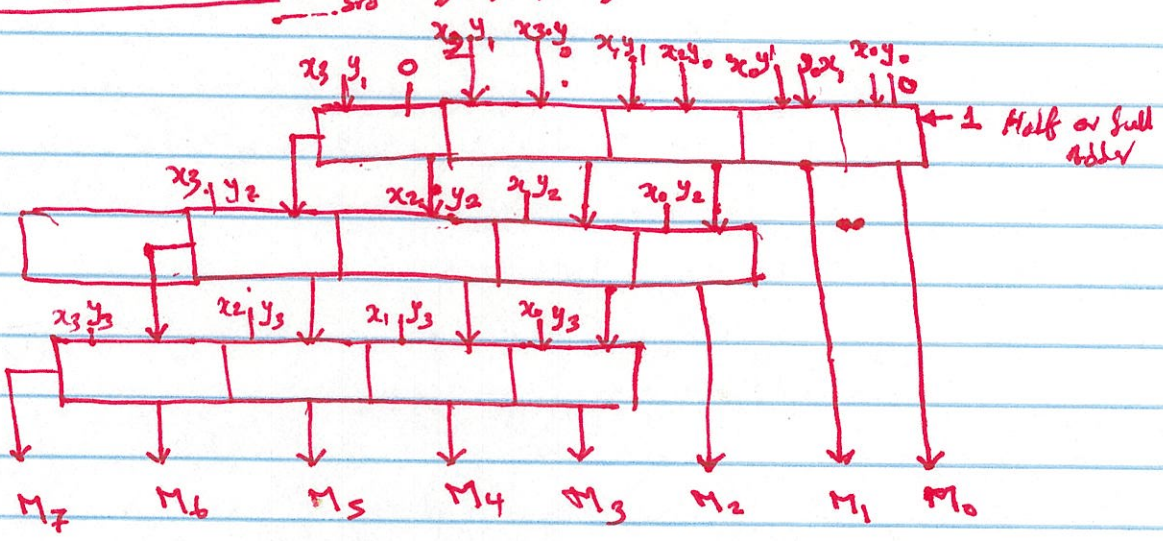
$0\quad x_3y_0\ \ x_2y_0\ \ x_1y_0\ \ x_0y_0$

$x_3y_1\ \ x_2y_1\ \ x_1y_1\ \ x_0y_1\quad$ "1"

$x_3y_2\ \ x_2y_2\ \ x_1y_2\ \ x_0y_2$ ---- 1st 5 bit adder

$x_3y_3\ \ x_2y_3\ \ x_1y_3\ \ x_0y_3$ ---- 2nd 5 bit adder

---- 3rd "



Delay = 7 MUX + 2 EX-OR + 1 AND = $7 * 1.5 t_g + 3 t_g = 13.5 t_g$ $\quad f = \frac{1}{13.5 t_g}$

Area = 16 AND + 13 1 bit Adder

Each one bit adder is $3A_g + 1.5A_g = 4.5 t_g$

Area = $16 A_g + 13 * 4.5 t_g$

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Q2

$A = 15.25_{10} = 1111.01_2 = 1.11101 * 2^3$ $e_A = 127+3 = 130$ $S_A = 0$

A packed | 0 | 1000 0010 | 11101000 ... |

$B = -0.75_{10} = -0.11_2 = -1.1_2 * 2^{-1}$ $e_B = 127 - 1 = 126$ $S_B = 1$

B packed | 1 | 0111 1110 | 1000 ... |

Exponent $e_A > e_B$ $exp\,A - exp_B =$

$e_B = 0\,111\,1110$ 2's Complement ...11000 0010 $-e_B$

$-01000\ 0010$

$00000\ 0100$ $e_A - e_B = e_R$

$e_A - e_B = 4$ shift significant of B by 4 bit to the right and Add to A

$01.11101 - 00.00011$ $\quad 001.11101 + 111.11101$

001.11010 $M_R * 2^4$

There is no need to normalize, No need to Round off

Pack the results

| 0 | 1000 0010 | 1101 .... |

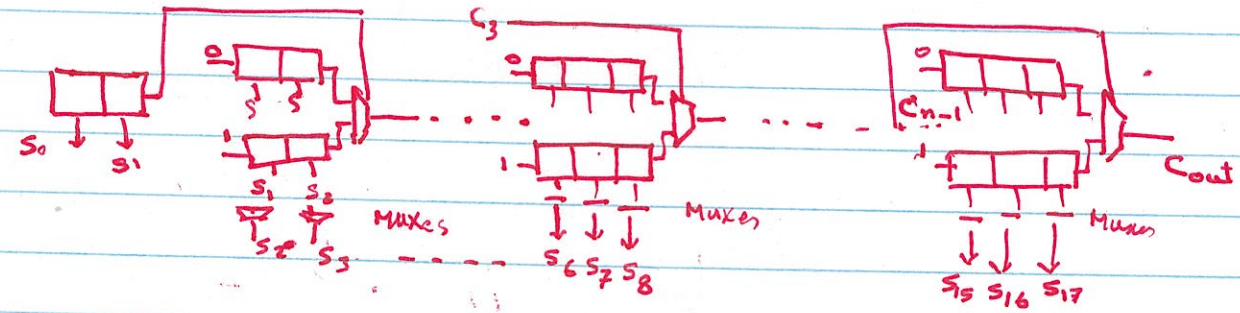
S_R e_r M_R

Architecture from Note

Q3

18 bits	Delay	Delay
2 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |		$6\tau_A$
2 2 | 2 | 2 | 2 | 2 | 3 | 3 |	or 33345	$5\frac{1}{2}\tau_A$
→ 2 2 | 2 | 3 | 3 | 3 | 3 |	{or 2222244 {or 1111122334 {or 333333 {or 44455	$5\ \tau_A$ Delay $5\tau_A$
2 2 | 2 | 4 | 4 | 4 |		$5\frac{1}{2}\ \tau_A$
4 4 | 5 | 5 |		$6\ \tau_A$

Within the selected combinations 2 223333 is selected



No. of full adders 34 Full adders
" " 2:1 Mux 22 Muxes

Area $= 34 A_F + \frac{1}{2} 22 A_F = 45 A_F$

Delay of 18 bit Ripple Carry Adder $= 3 \times 6 = 18\tau_A$

Area " " " " " $= 18 A_F$

Ripple Carry Adder