FPGA Timing Models

- Most FPGA and CPLD vendors provide a *timing model* in their data sheets that allow estimation of path delays.
- Some example path delays that are of interest:
  - Minimum Pin to Pin delay
    - (through input pin, through one combinational logic element, through one output pin.)
  - Minimum Register to Register Delay
    - .From clock input pin, through global net . through Clock to Q delay through DFF of a logic element, through one combinational logic element to setup time on DFF input).

FPGA Timing Models (cont)

- These timing models allow estimations of maximum attainable performance
- Some vendors use their timing models as selling points
  - Simpler is better - easier to estimate timing from a simple model than a complex one.
  - Routing delays will always complicate the timing model
- After a design is mapped to an FPGA or CPLD, always must use a static timing analysis program to compute the timing performance.

Actel MX C-module (Combinational Module)

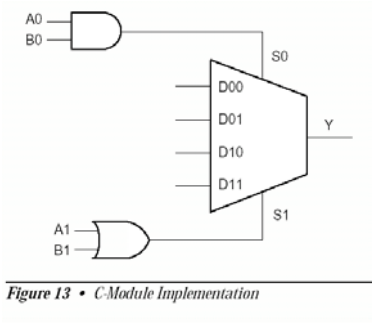
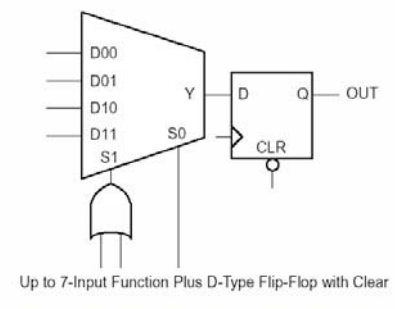


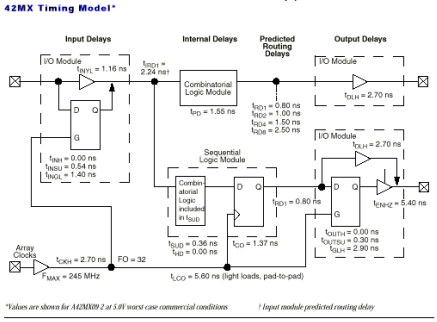
Figure 13 • C-Module Implementation

Actel MX S-module (Sequential Module)



Up to 7-Input Function Plus D-Type Flip-Flop with Clear

Actel 42MX Timing Model



Pin to Pin delay Example

Input pad through combinational element through output pad

From timing model:

$T_{INYL} + T_{IRD1} + T_{PD} + T_{RD1} + T_{DLH}$

1.16ns + 2.24 ns + 1.55ns + 0.8 ns + 2.7 ns

Pin to Pin = 8.45 ns

T_{INYL} Input pad to Y low
T_{IRD1} Input Fanout 1 routing delay (higher the fanout, longer the delay)
T_{PD} Logic module prop delay
T_{RD1} Output Fanout 1 routing delay
T_{DLH} Data to Pad high delay

Environment affects Timing

Actel uses derating factors for timing values. A derating factor is a multiplication factor applied to the timing value.

42MX Temperature and Voltage Derating Factors (Normalized to T_J = 5V, 25 °C)

42MX	–55	–40	0	25	70	85	125
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Notice that fastest timing (smallest derating factor) is for high Voltage, low temperature. The slowest timing (largest derating factor) is for low voltage, high temperature.

Four corners: (low temp, low vdd), (high temp, low vdd), (low temp, high vdd), (high temp, high vdd).

Processing Variations can also affect Timing

Timing can vary from one batch of wafers to another due to process variations. There are also *four corners* for processing variations: (fast-p, fast-n), (slow-n, fast-n), (fast-p, slow-n), (slow-p, slow-n). 'fast-p','slow-p' refer to fast pmos transistors, slow pmos transistors. 'fast-n', 'slow-n' refer to fast nmos transistors, slow nmos transistors, respectively.

Data sheets use timing variations due to processing to determine the speed grades; Voltage/Temperature derating factors are then applied to individual speed grade timings.

Actel specifies a 0.45 derating factor for best case processing. This would be important if you were trying to compute the minimum delay.

Speed Grades

- Important to realize that speed grades are determined via the timing variations due to processing
  - There are no functional differences between speed grades.
  - A functional difference would require a different part number.
- Vendors will charge premium prices for the best speed grade parts