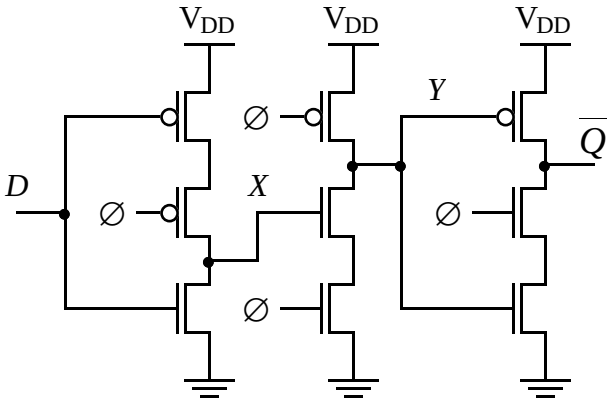
Observations for other Positive Edge-Triggered D-FF

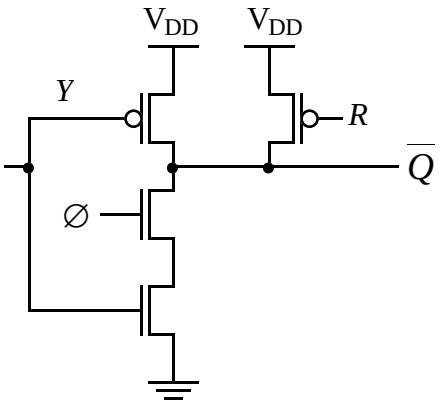


positive edge-triggered TSPC D-flip flop (non-split output)

Need to analyze for clock = 0 (master sampling, slave holding), clock 0 → 1, clock = 1:

clock	D	X	Y	$\overline{Q}$
0	0	1	1	$\overline{Q}_{old}$
0	1	0	1	$\overline{Q}_{old}$

Need to force $\overline{Q}_{old}$ to a "1". Can do it by → → → → → → → → →

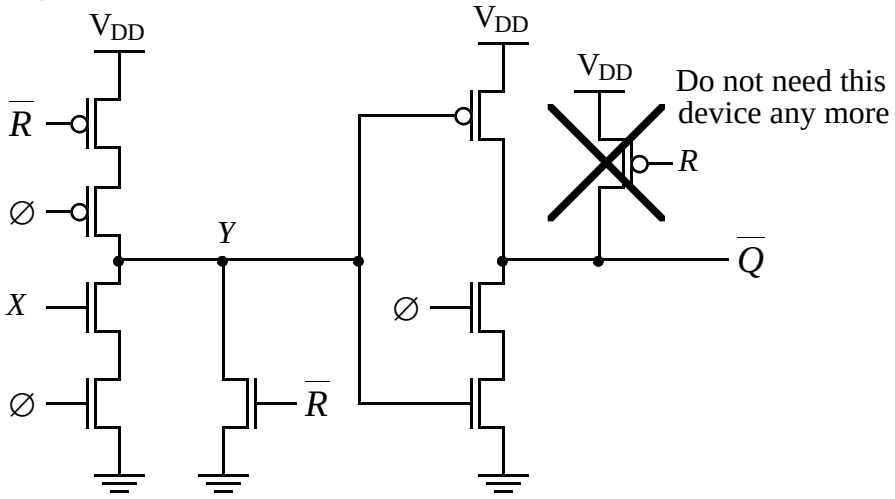


Check other cases:

clock	D	X	Y	$\overline{Q}$
0 → 1	0	X_{old} (= 1)	0	1
0 → 1	1	X_{old} (= 0)	Y_{old} (= 1)	0

For the above case where clock is going 0 → 1 and D = 0, no reset is needed. In the second case above where clock is going 0 → 1 and D = 1, we need to force Y_{old} to be a <u>zero</u> when reset is asserted. How to do this?

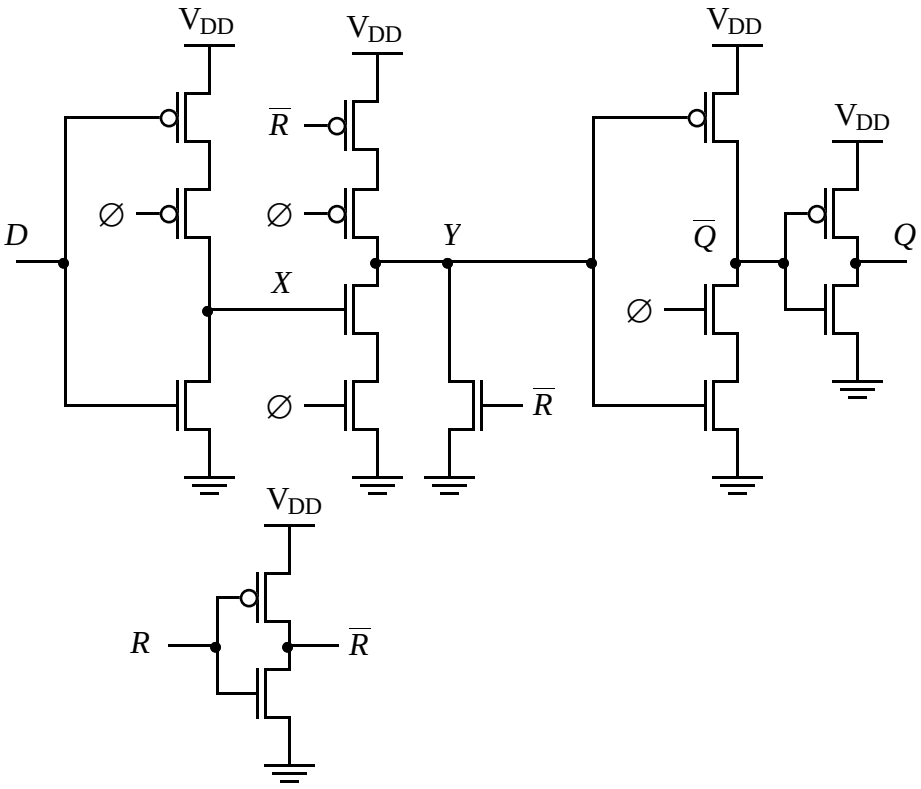
Here's one way:



When clock ($\varnothing$) = 0 $\rightarrow$ 1, R = 0, $\overline{R}$ = 1, then forces Y node = 0. Even works when clock = 0, can get rid of *p*MOS pullup on $\overline{Q}$ output.

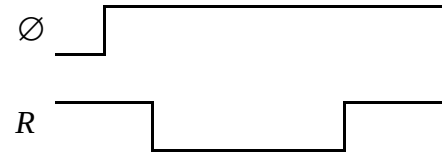
Will have to invert $\underline{R}$ inside of circuit because R is low true, so final transistor count for adding asynchronous low true reset is $\underline{4}$.

Final circuit (positive edge-triggered TSPC *D*-flip flop with asynchronous, low-true reset):

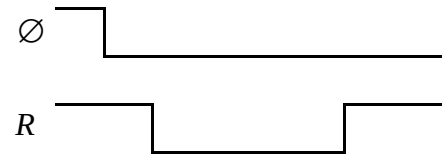


Final transistor count = 15. Recall again that a static *D*-flip flop can require 33 transistors!

Final check →



$X = X_{old}$ $Y = Y_{old}$
$Y = 0$ $\overline{Q} = 1$
$\overline{Q} = 1$



$X = \overline{data}$ $Y = 1$
$Y = 0$ $\overline{Q} = \overline{Q}_{old} = 1$
$\overline{Q} = 1$