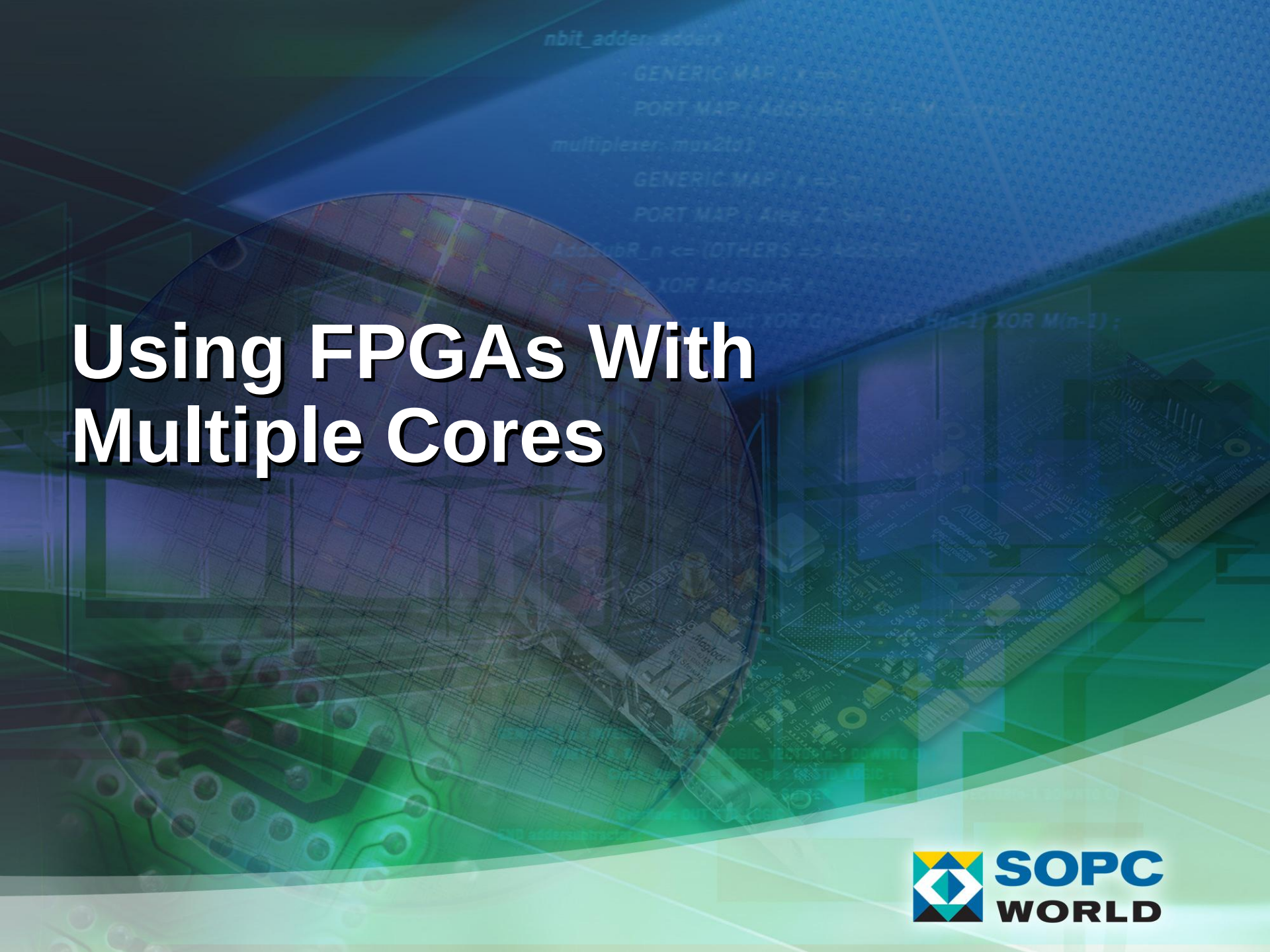

Using FPGAs With
Multiple Cores
SOPC
WORLD

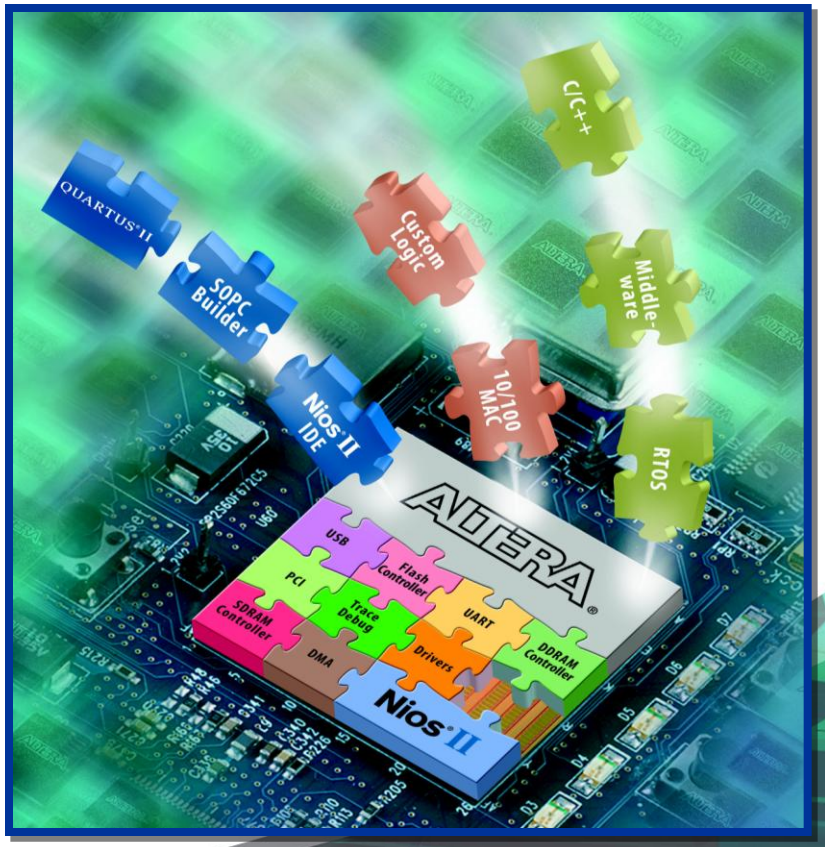
# Agenda

- Background: FPGA-based computing
- FPGA computing topologies and scalability
- Hardware acceleration
- Effect of multiple cores on productivity
- Conclusion
- Q&A

# Background: FPGA-Based Computing

# Today's FPGA Devices Meet Advanced System Requirements

- Wide range of fast I/O
- Substantial embedded memory
- High-performance digital signal processing (DSP) blocks
- Abundant logic
- Low-cost FPGA and structured ASIC families



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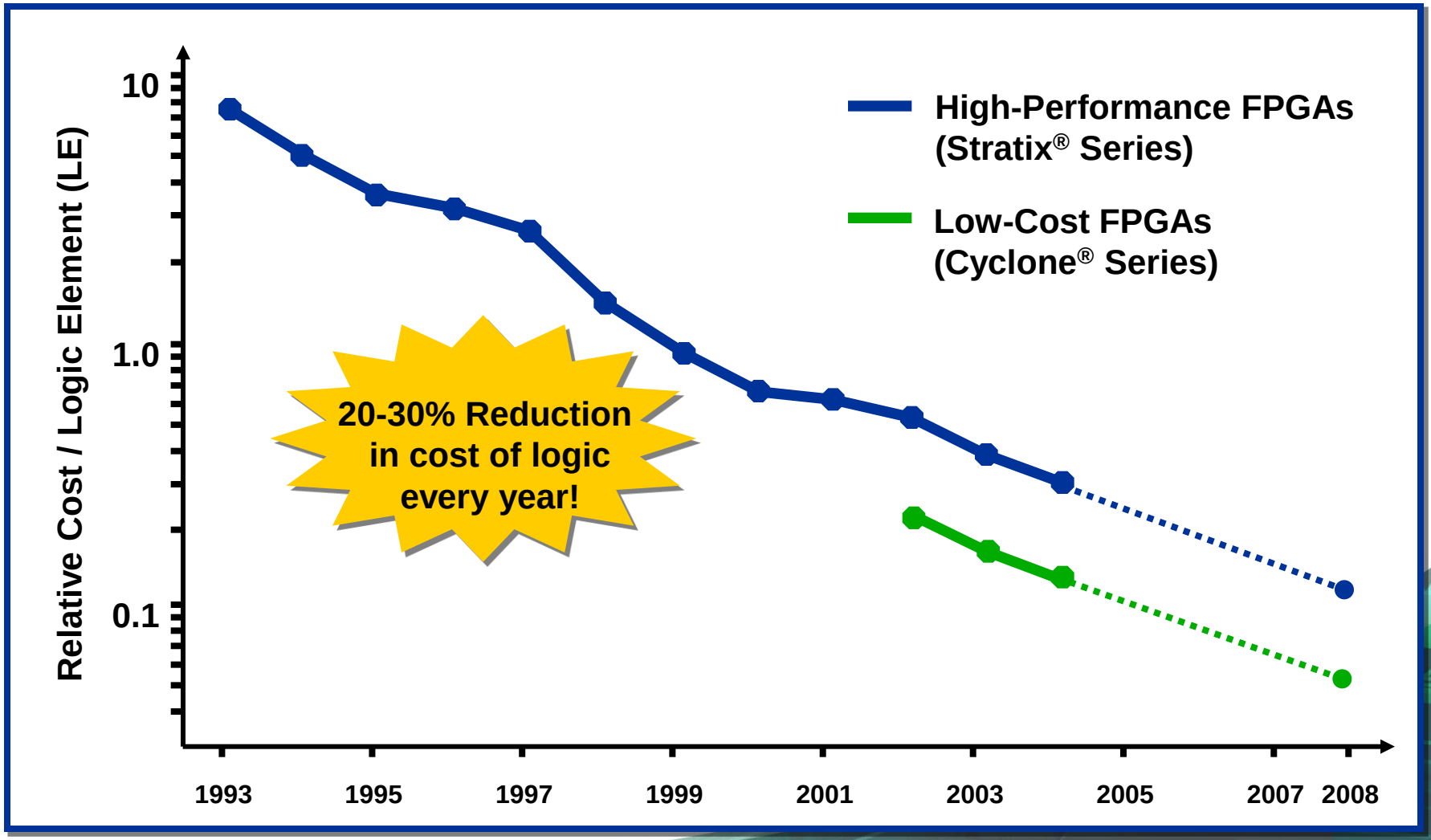
# FPGA-Based System Economics



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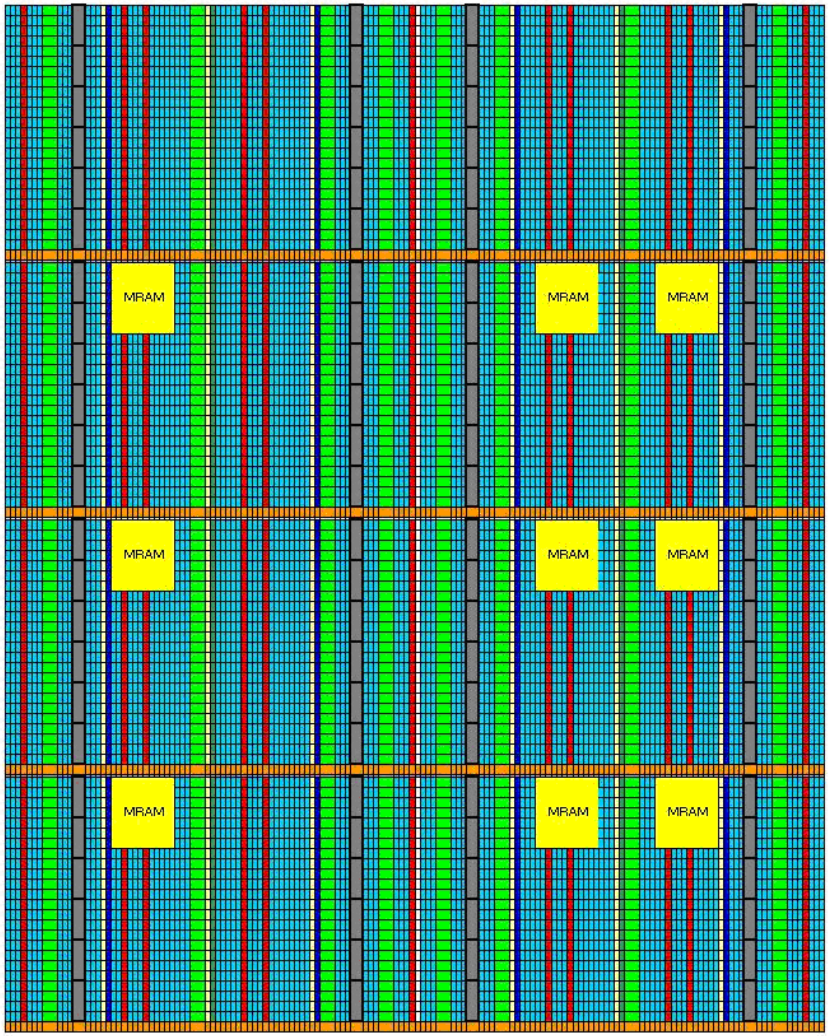
# Modern FPGAs: Platforms for High-Performance Parallel Architectures




- Example: Altera's Stratix II Family
  - First 90-nm high-end FPGA
  - TSMC Fab
  - Shipped in June 2004
- Rich interconnect fabric
- Up to 180K LEs
- Up to 9 million memory bits
- Up to 96 flexible DSP blocks
- Up to 1,170 high-speed I/O pins
- Many clock trees and phase-locked loops (PLLs)



SOPC WORLD

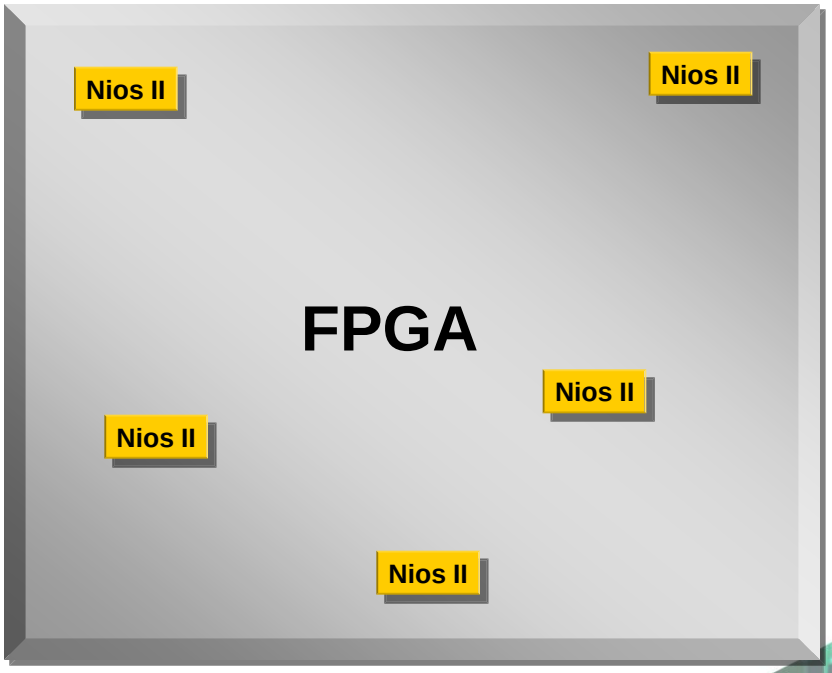
# Soft-Core CPUs Are Affordable

**Small Cyclone II**
**4,600 Look-up Tables (LUTs)**


**600 LEs**
**13% of FPGA**
**Nios II/e "Economy"**

**35¢ in**
**Lowest-Cost**
**FPGA**

**Largest Stratix II**
**180,000 LUTs**




**1800 LEs, 1% of FPGA**
**Nios II/f "Fast"**

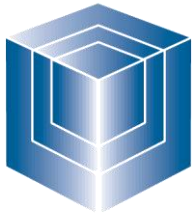


SOPC WORLD

# FPGA = Fast Development

- Fast time to production
  - Prototype and production boards can be the same
  - Can accommodate late changes
  - Use/reuse intellectual property (IP)
- Fast design cycle
  - Develop → synthesize → test
- System-level design tools
  - Integration of IP and in-house designs
- Powerful system debug tools
  - Software and hardware

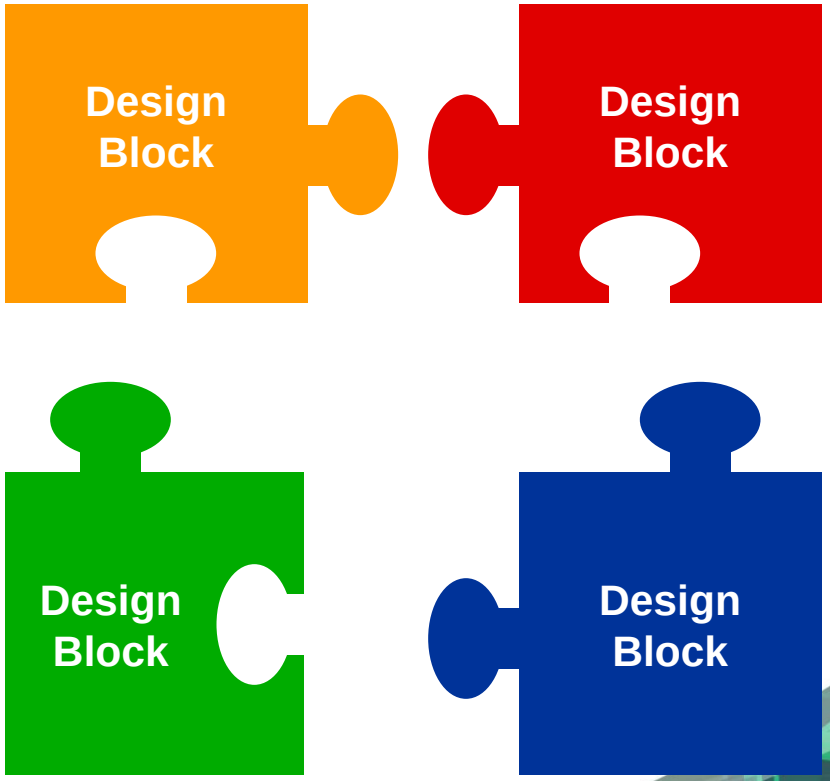






# Using IP to Increase Productivity

- Not all blocks are designed with the same interface
- Design for reuse can lead to greater time and cost
- Blocks need integration to create system



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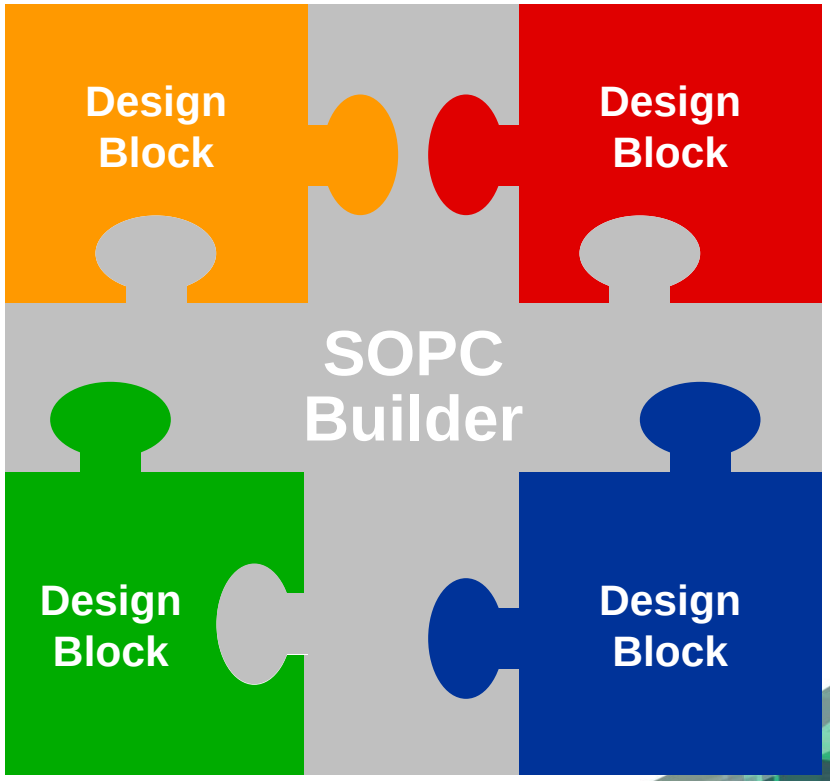
# SOPC Builder - Automated Integration

- Generates interconnect between IP blocks
  - Supports third party and in-house IP
- Automatically resolves interface issues
  - Clock domains
  - Bit widths
  - Arbitration
  - Other issues

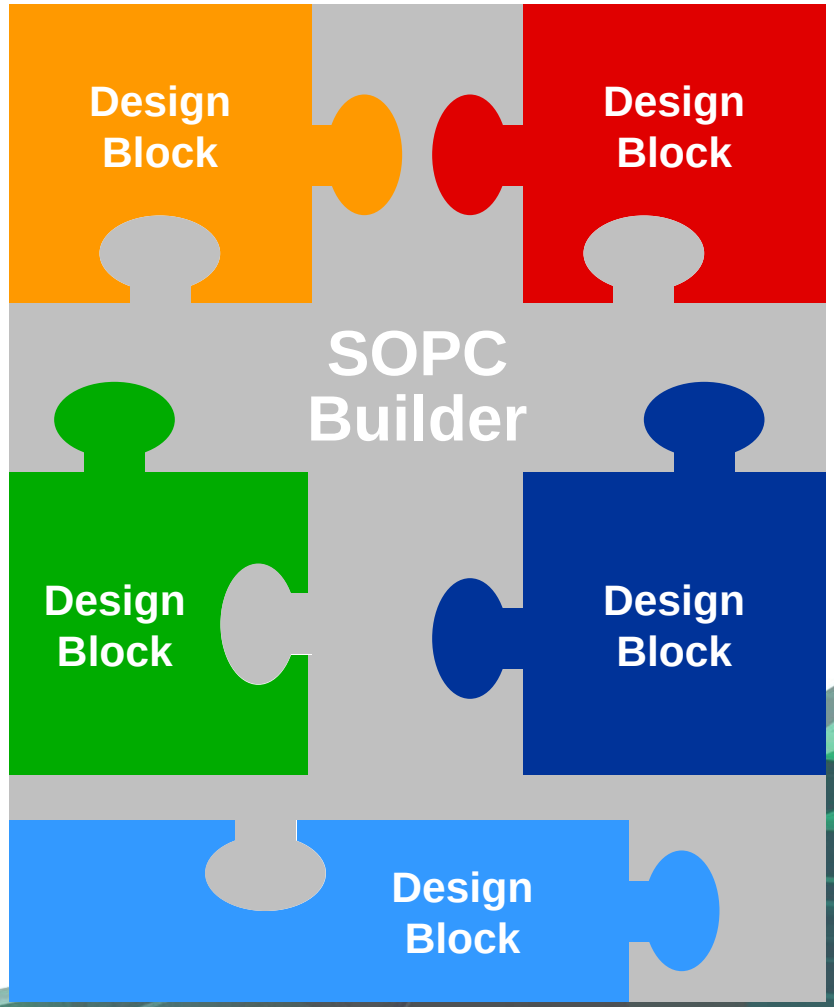





SOPC WORLD

# Updating the System

- SOPC Builder systems can be easily extended
- No need to “hack” into existing system
- Minimal disruption to the rest of the system



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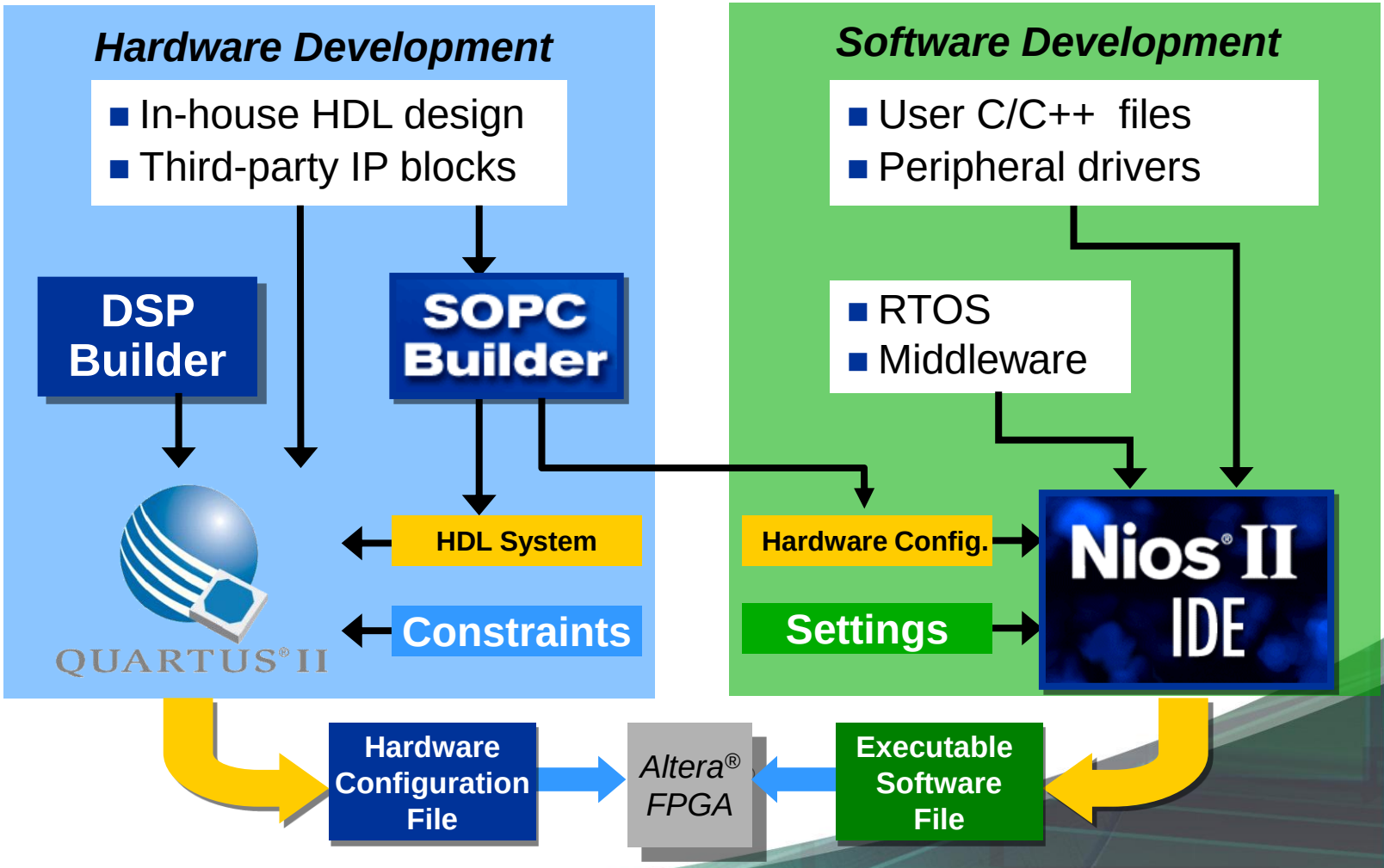
# Embedded System Design Flow



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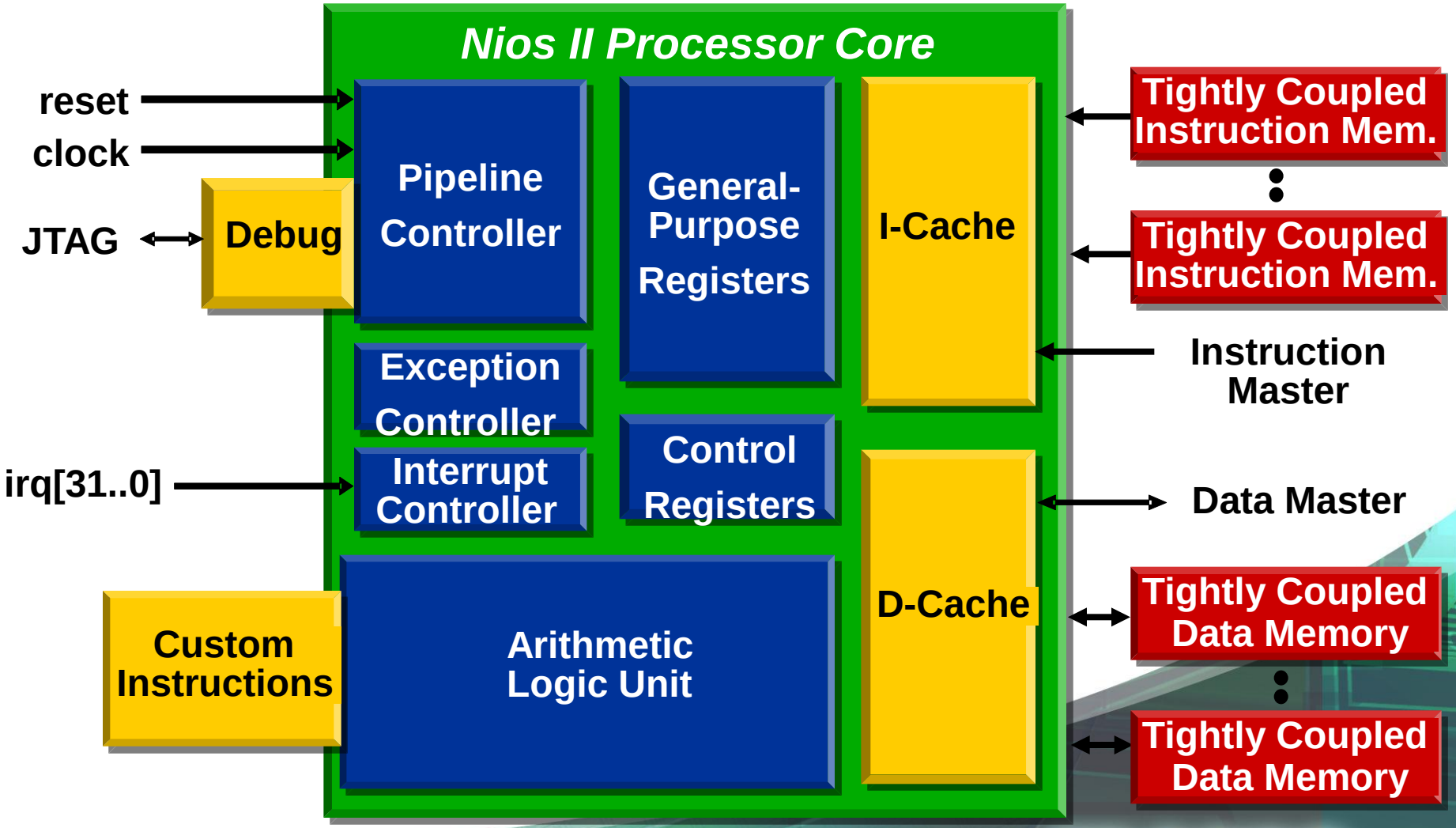
# FPGA-Based Soft CPU: Nios II



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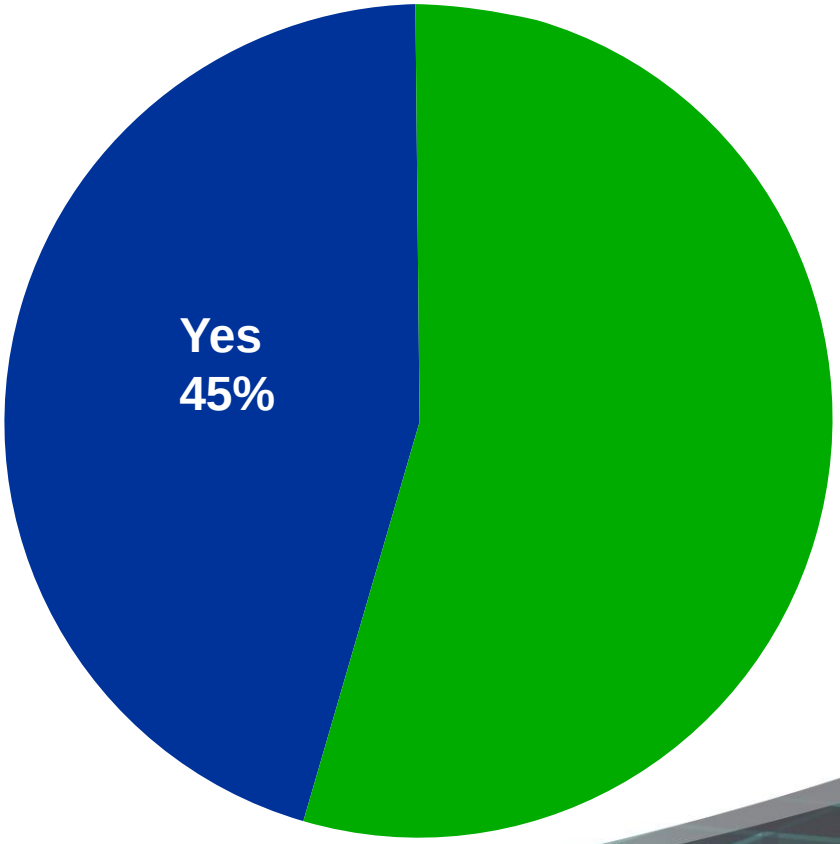
# FPGA-Based Soft CPU Usage Trend

Percent of EE Times embedded systems designers who say they "will likely use a processor inside an FPGA"




Source: CMP 2005 Embedded Market Study



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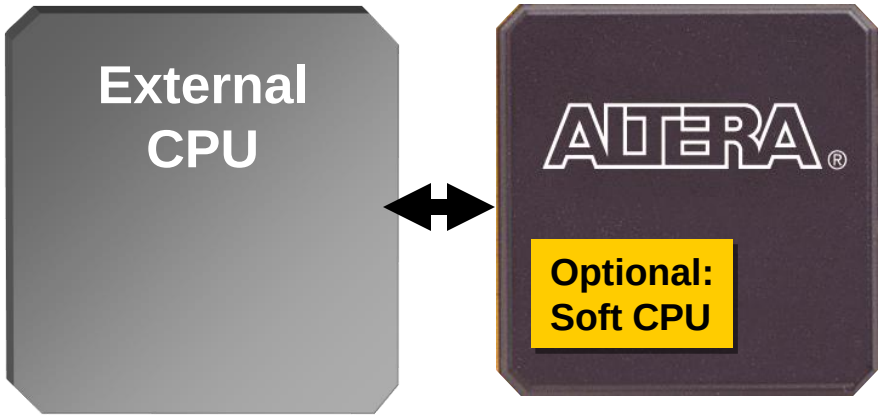
# FPGA Computing Topologies

# Two FPGA Computing Topologies

## *Standalone Computing*


## *Companion Computing*

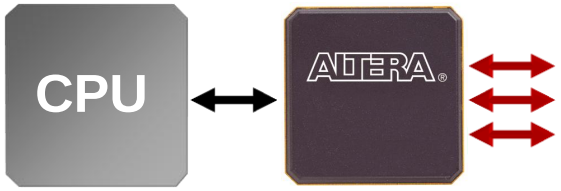





SOPC WORLD

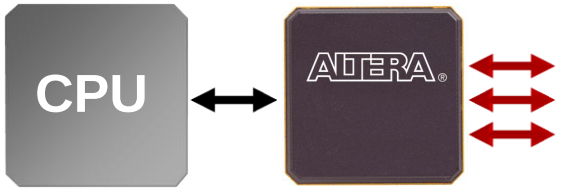
# Enhancing Your System With FPGAs

- Peripheral expansion
  - Extends life of CPU
  - Enhances flexibility
  - Avoids costs and risks of using new part

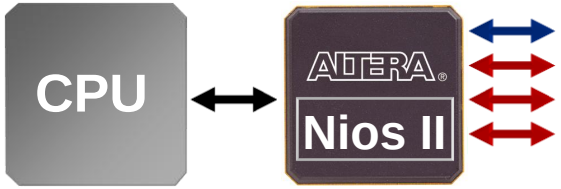


# Enhancing Your System With FPGAs

- Peripheral expansion




- CPU offload
  - No increase in clock speed
  - Preserves real-time set up
  - Low power consumption
  - No upgraded components required
  - Increases flexibility



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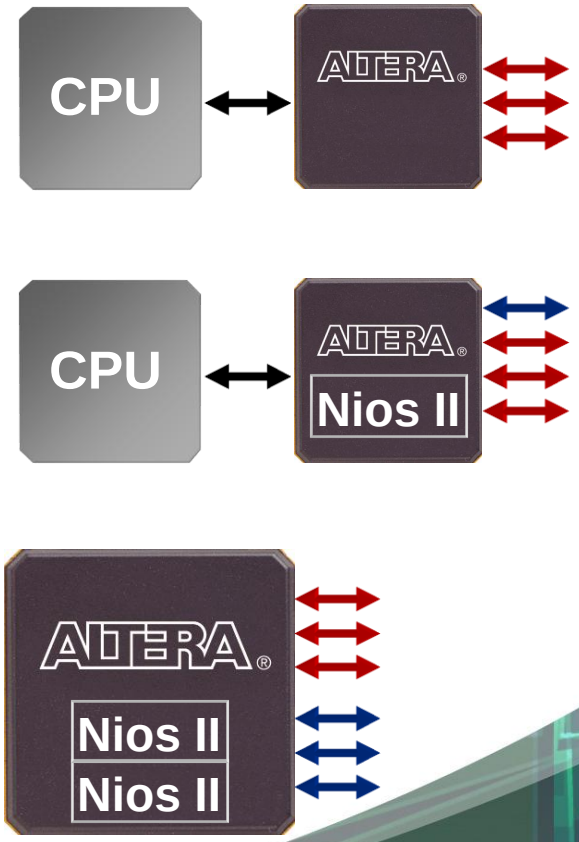
# Enhancing Your System With FPGAs

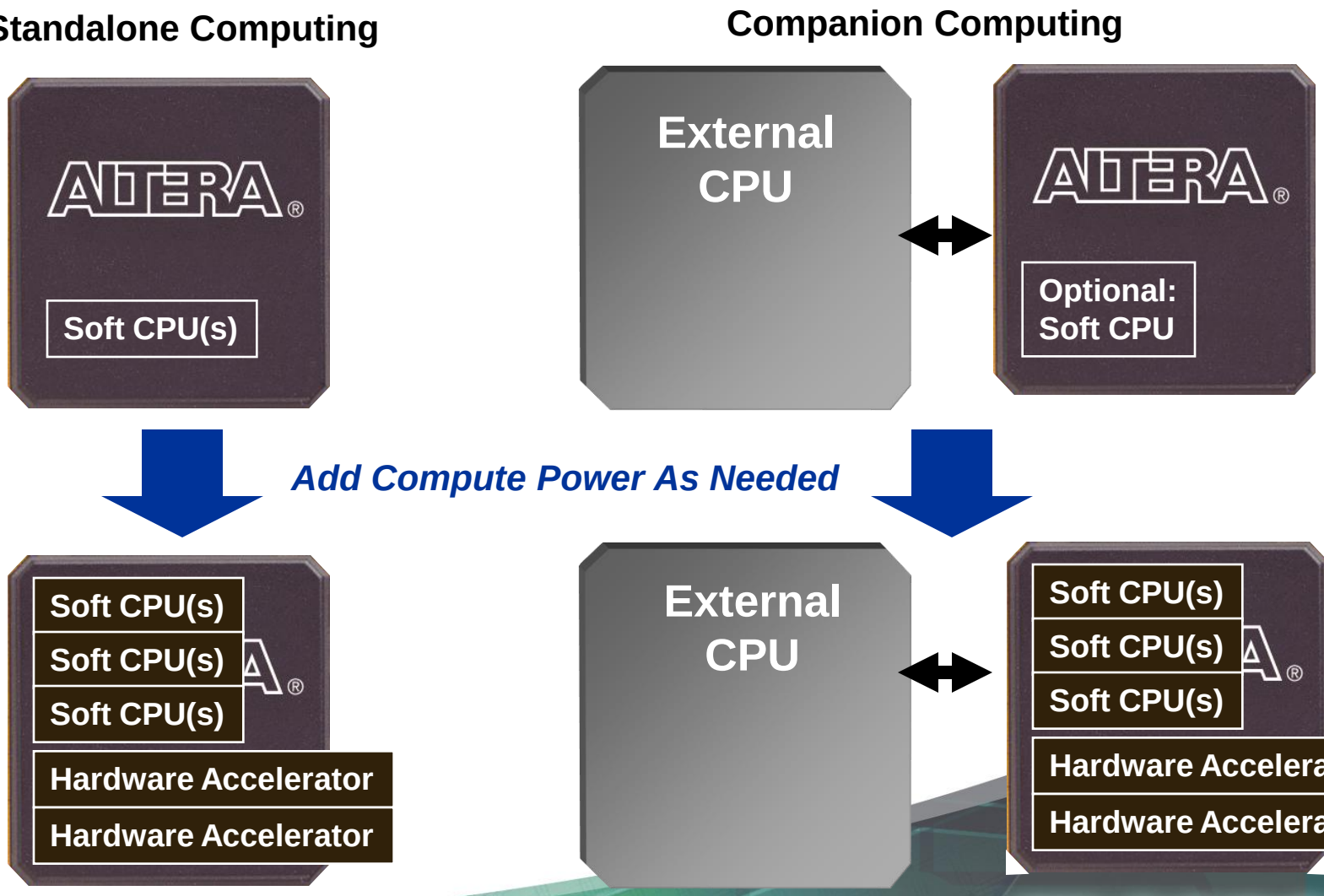
- Peripheral expansion
- CPU offload
- Full system integration
  - Very flexible
  - Fast development
  - No obsolescence issues
  - High performance/low cost






SOPC WORLD

# Multiple-Core Scalability

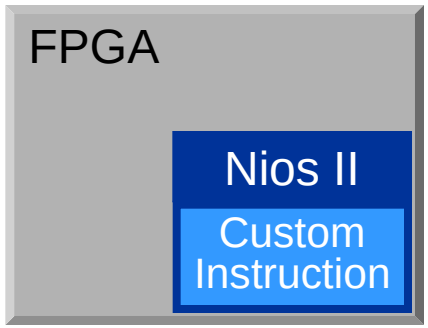





SOPC WORLD

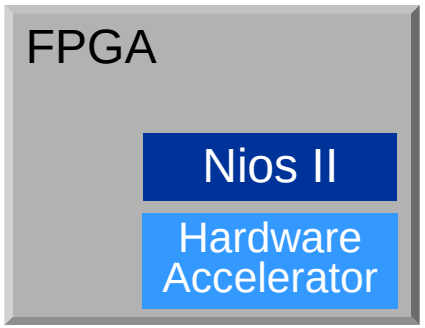
# Three Ways to Scale Performance

## Custom Instructions



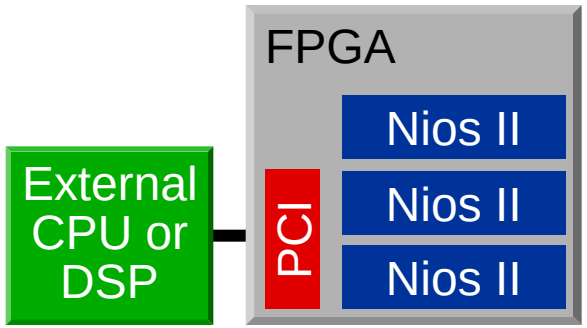

- Accelerate CPU processing performance with application-specific hardware

## Hardware Accelerators




- Add external coprocessing hardware to accelerate data functions

## Multiprocessor System




- Add more processors (internal and/or external) to increase processing power



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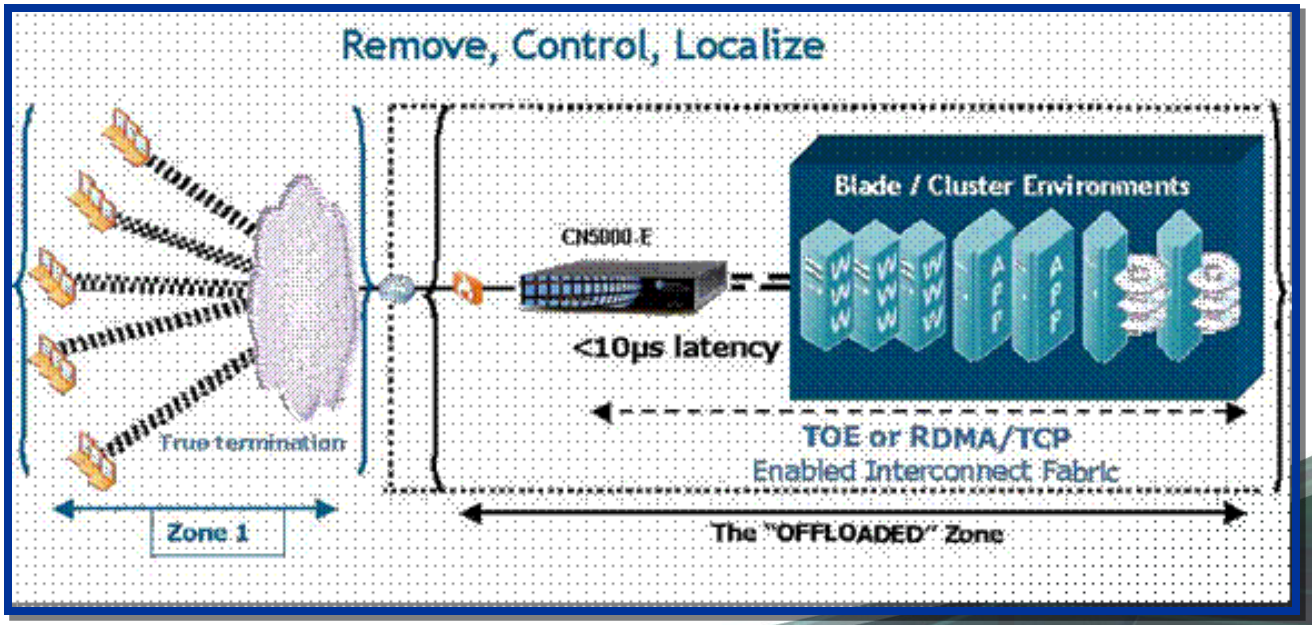
# Multi-Channel Processing

## Crescendo *Maestro CN-5000E*


**Application:**

Application Acceleration Platform





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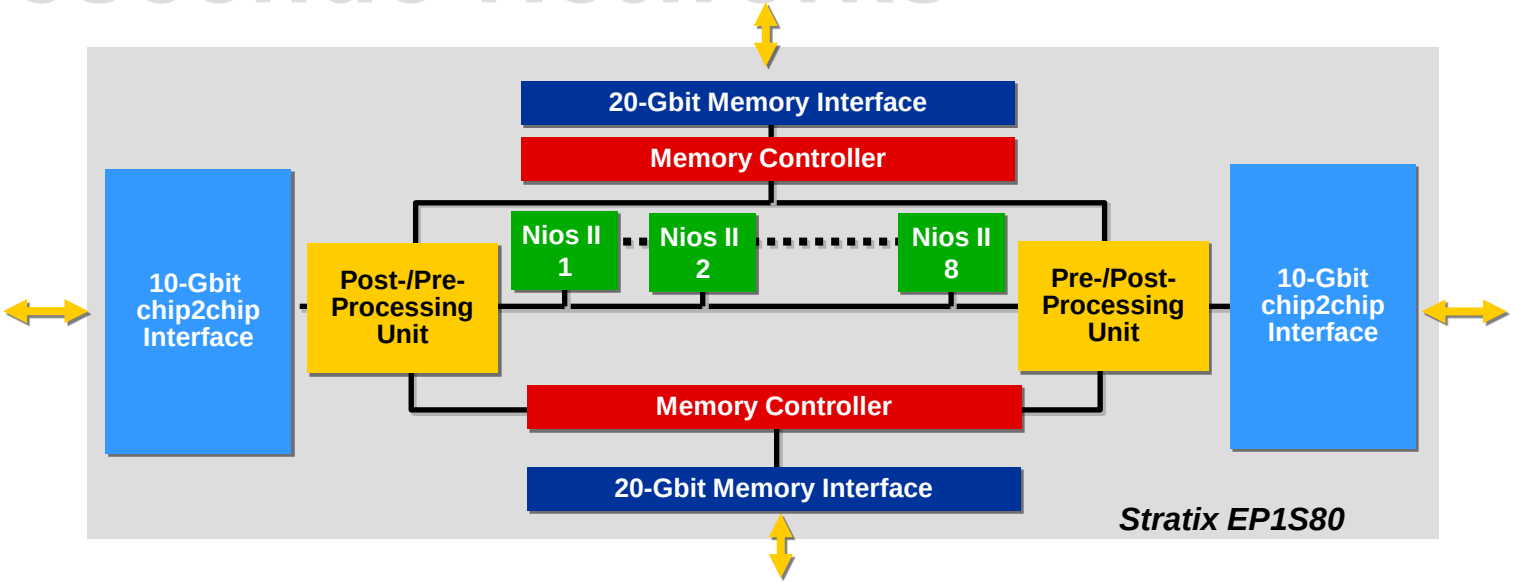
# Crescendo Networks




- Eight Nios II Processors
  - TCP/IP offload engine (TOE)
  - Complex memory management
  - Header parsing

- Comparisons
  - ASIC
    - Lower development cost
    - Faster time to market
  - ASSP
    - More flexible
  - Off-the-shelf processor
    - Able to support multi-Gbit bandwidth

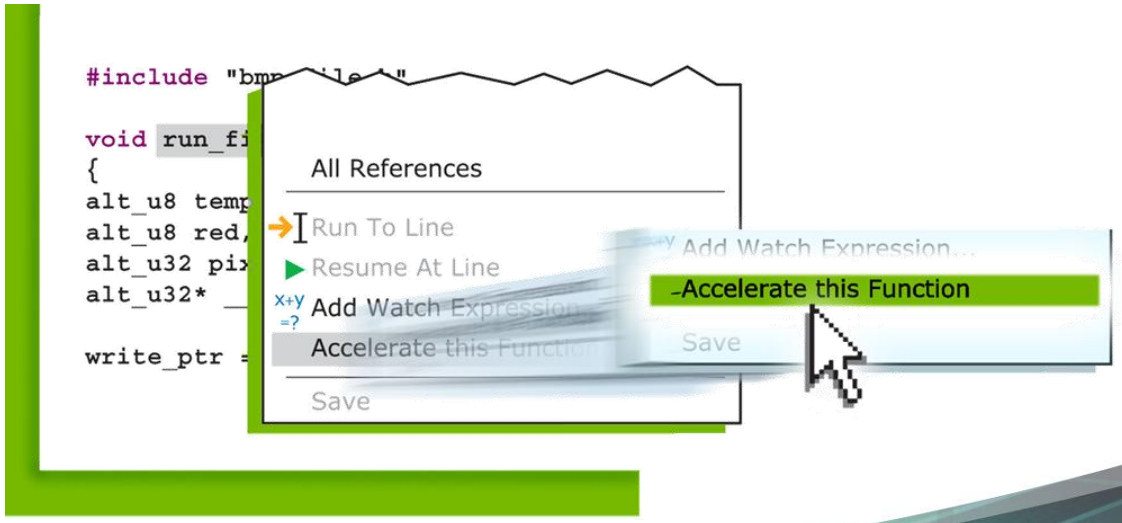


SOPC WORLD

# Hardware Acceleration

# Advanced C-to-Hardware Acceleration (C2H) Productivity Tool

- Automates creation and integration of hardware accelerators
- Intuitive user interface streamlines C acceleration
- Uses familiar Nios II Integrated Development Environment (IDE)
- Support for standard ANSI C language




**Right-Click to *Accelerate***



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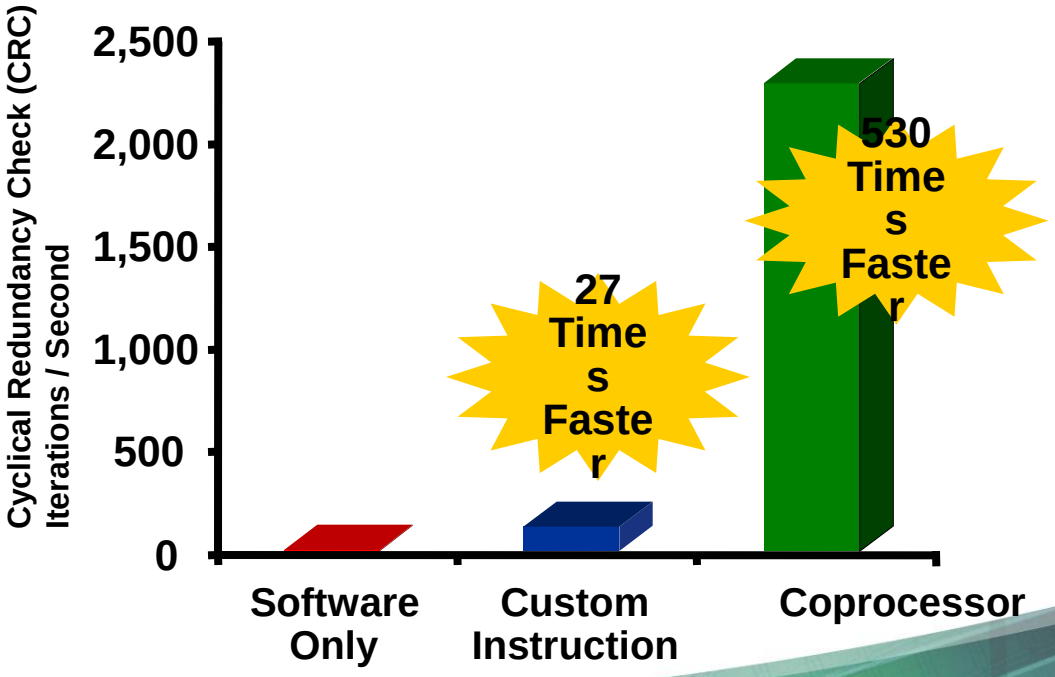
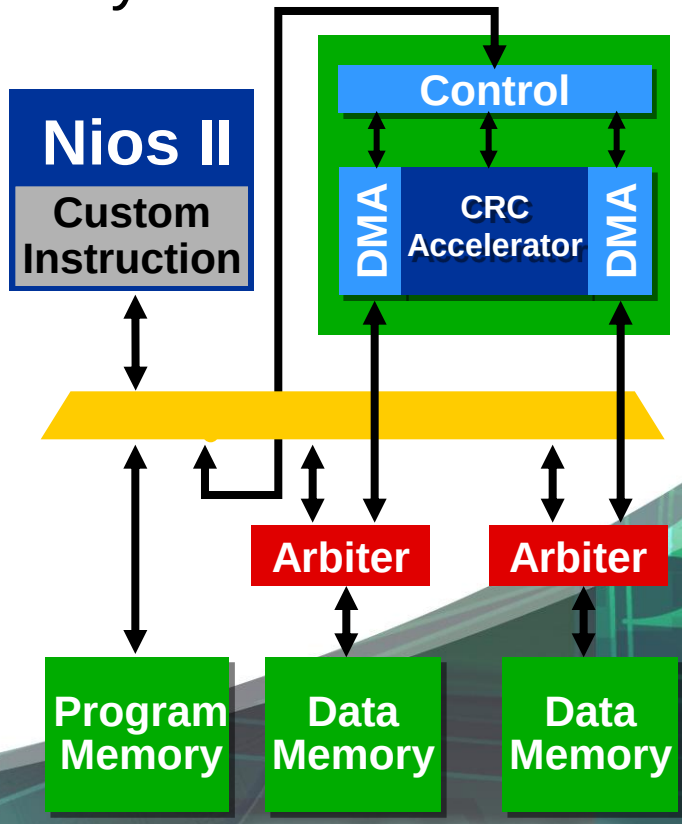
# Add Hardware Accelerator

- CPU starts/stops accelerator
- Accelerator fetches data and stores results
- CPU runs application code concurrently
- Ideal for block data operations



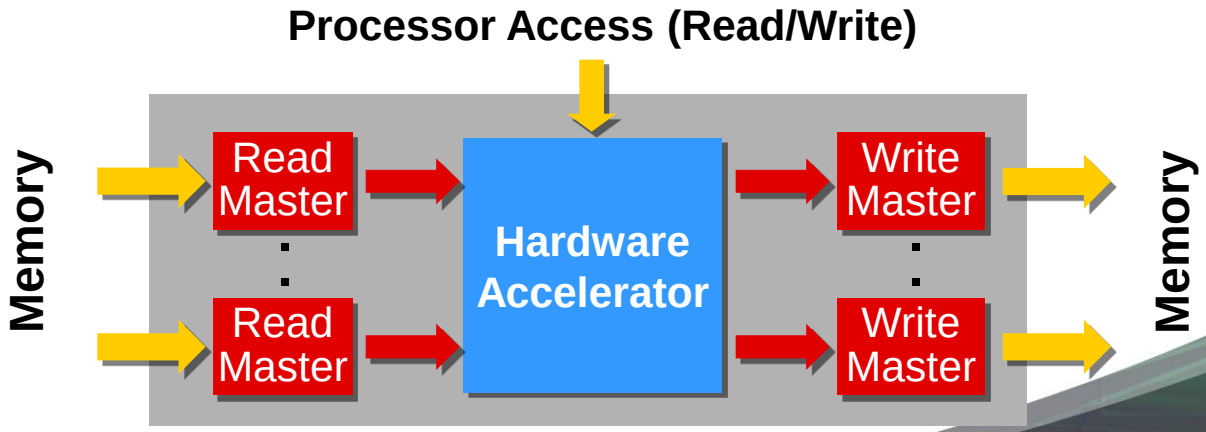

* Processor running at 100 MHz



SOPC WORLD

# Anatomy of a Hardware Accelerator

- Multiple Avalon® master interfaces to memory
  - Accelerator pipelined to match memory latency
  - Can sustain extremely high throughput
- Slave interface for CPU control
  - Memory mapped registers such as configuration, start, stop, status, etc.
- Software wrapper function
  - Controls hardware via slave interface



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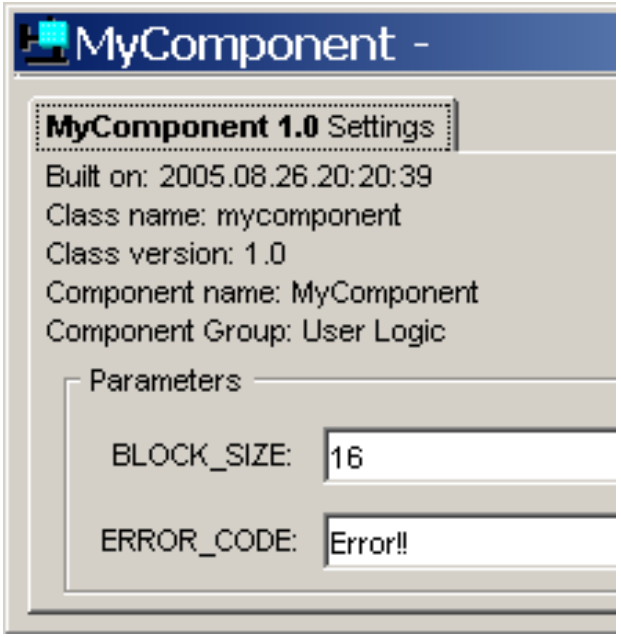
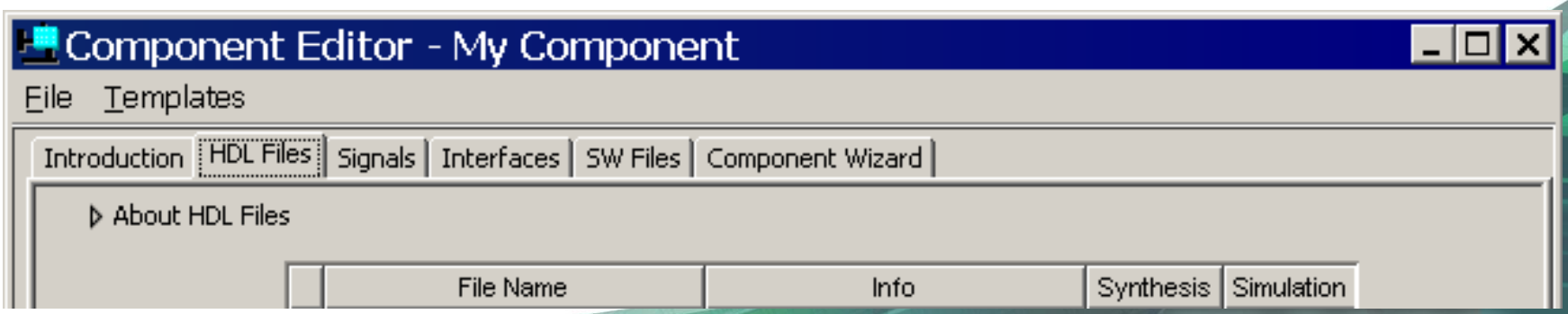
# Adding SOPC Builder Components

- Import hardware design files
- Map signals to Avalon switch fabric
- Set additional timing parameters
- Add software files (optional)
- Add component information
- Add to SOPC Builder library



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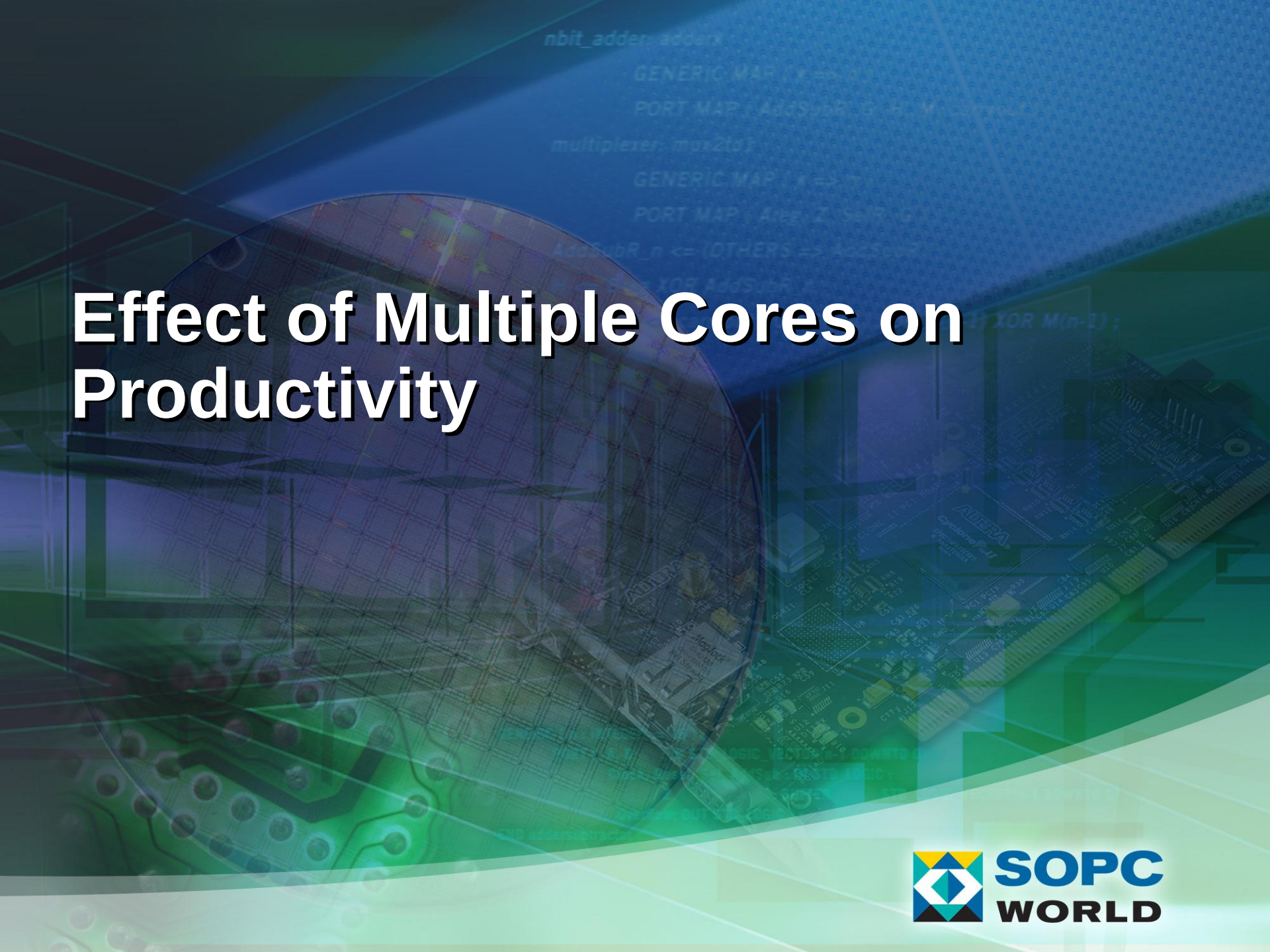
# Performance Comparison

- Mandlebrot algorithm
  - Pentium M running 1,600 MHz, entirely out of cache (best case)
  - Cyclone II system running Nios II processor at 75 MHz with acceleration blocks

| | Floating-Point Software | Integer Software | Accelerator Hardware | Direct Memory Access (DMA) I/O Offload Hardware |
|---|---|---|---|---|
| Pentium at 1,600 MHz | **30 ms** | 110 ms | NA | NA |
| Pentium at 75 MHz | 640 ms | 2347 ms | NA | NA |
| Nios Processor at 75 MHz | 351,789 ms | 243,017 ms | 211 ms | **35 ms** |

# Effect of Multiple Cores on Productivity



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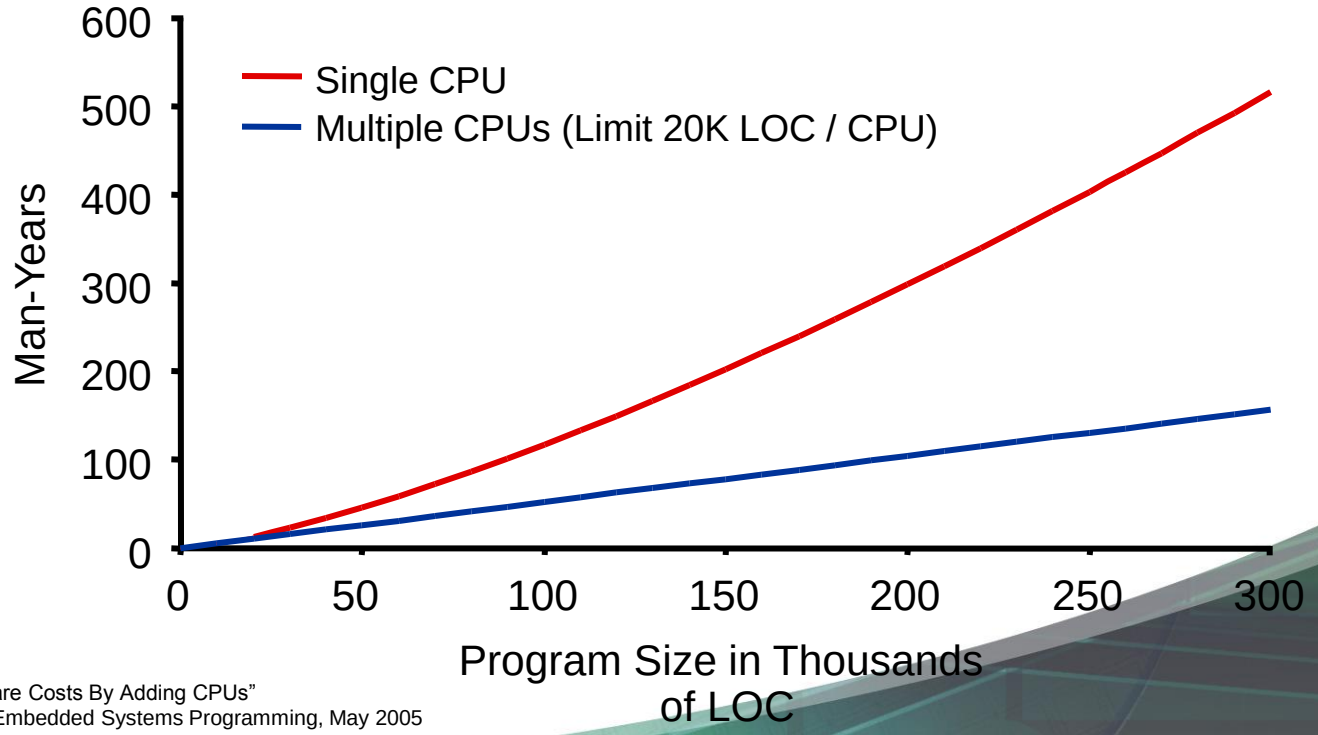
# Multiple Cores Drive Team Productivity

- Each processor runs fewer lines of code
- Smaller projects are faster to develop
  - "Double the lines of code (LOC) and multiply man-months by four" *
- Improves reliability and maintainability
  - Large function error rates 2X to 6X higher than smaller routines **




* "Subtract Software Costs By Adding CPUs"
-- Jack Ganssle, Embedded Systems Programming, May 2005

** "An Empirical Study of Operating System Errors"
-- Chu, Yang, Chelf, Hallem, Proceedings of the 18th ACM Symposium on Operating System Principles, October 2001



SOPC WORLD

# Multiprocessor System Design Made Easy

- Building multiple-CPU systems with SOPC Builder
  - As many Nios II CPUs as you like
  - Communicate via shared memory mailbox
  - Share hardware resources with mutex core
- Software development:
  - Integrated drive electronics with multiprocessor debug support
  - Software drivers for mailbox and mutex
  - Enhanced tool support from Lauterbach
- Example designs and application notes



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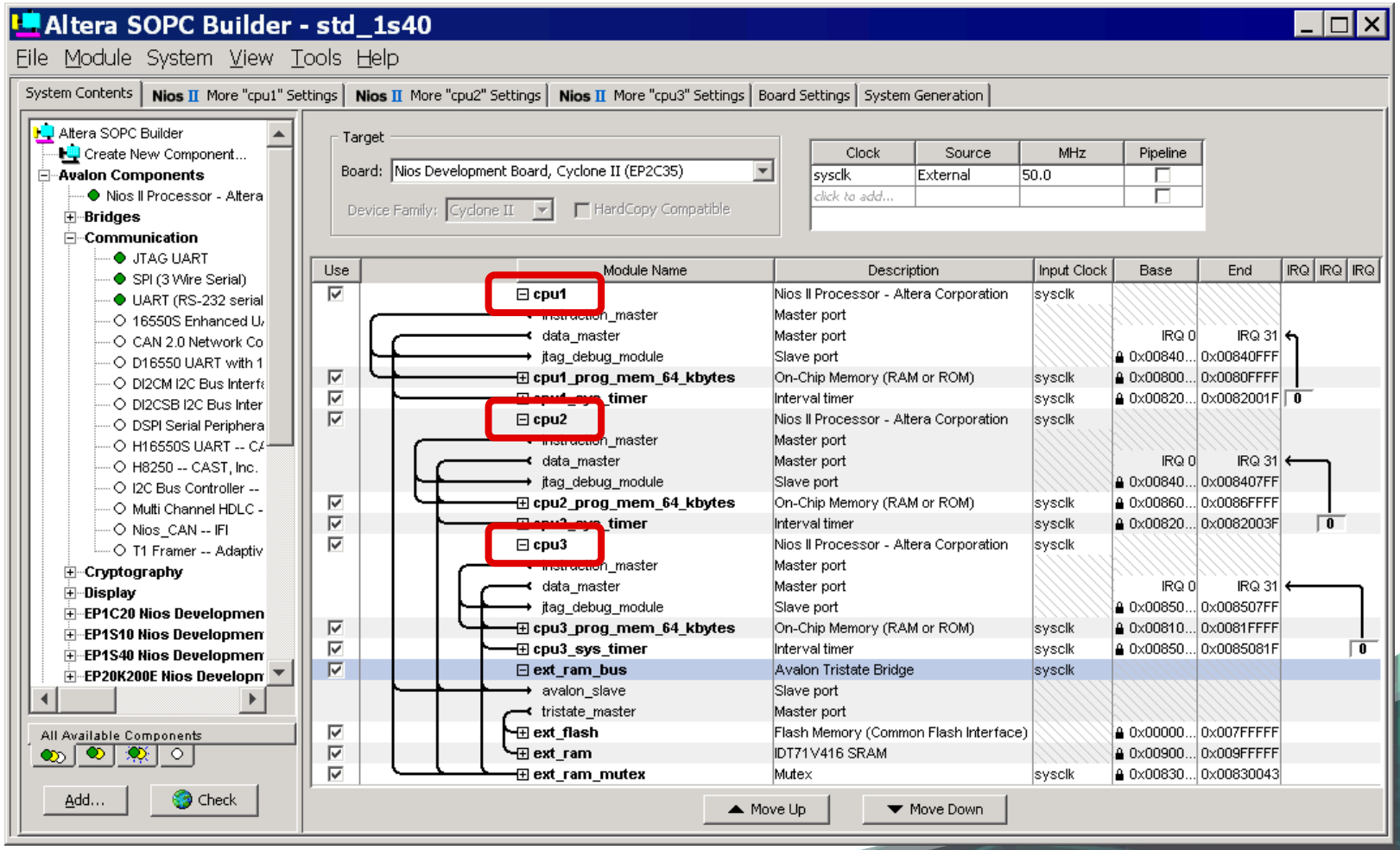
# Nios II Multiprocessor System



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# Benefits of Multiprocessor Design

- Can increase performance
  - More work per clock cycle
- Can scale system design
  - Add CPU when required
- Can reduce cost
  - External processor upgrade not required
- Can simplify software development

# Conclusion

# Conclusion

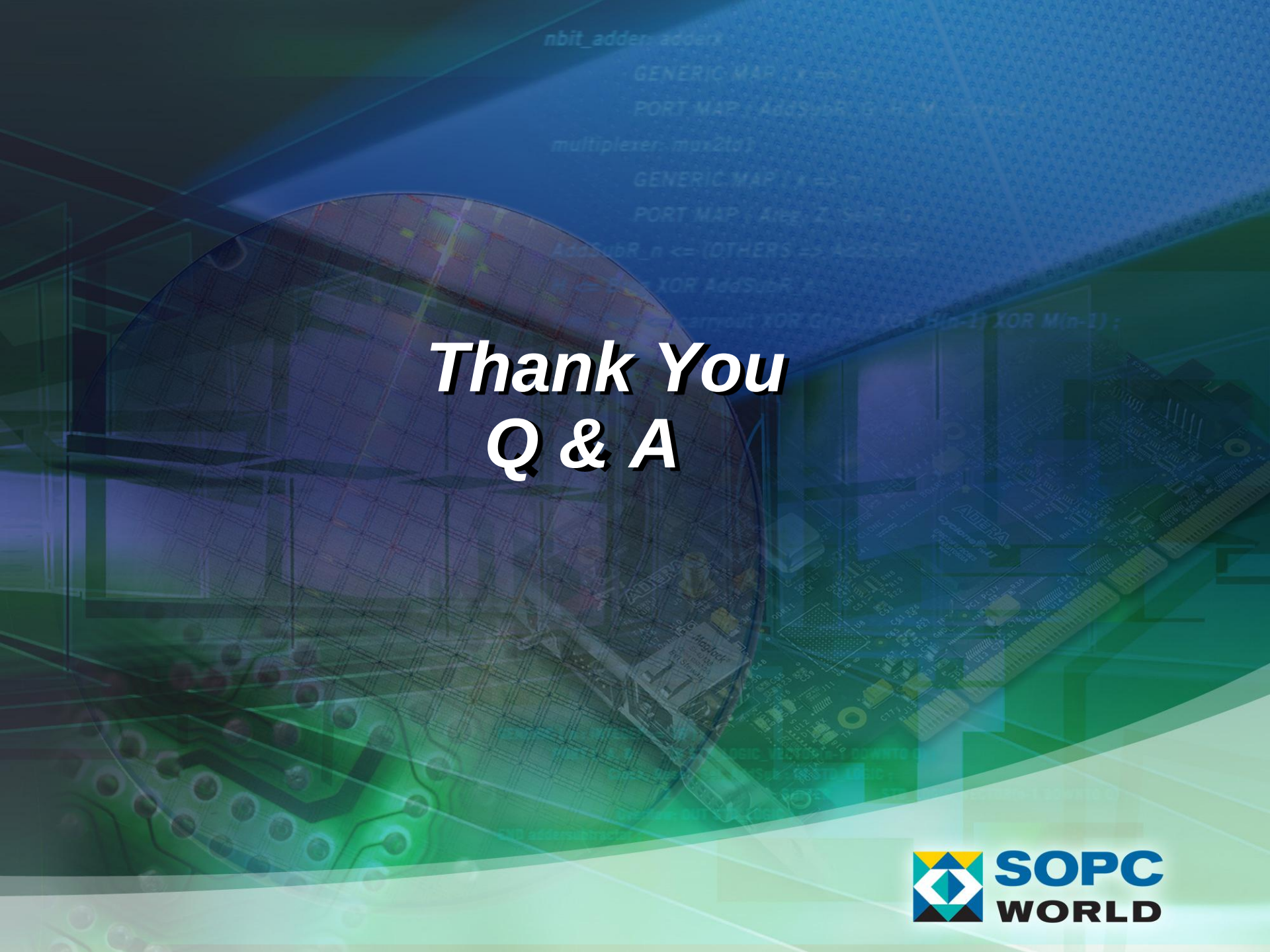
- FPGAs can be viewed as a flexible, scalable computing platform
- FPGAs support general and specialized computing cores
- FPGA-based soft CPU cores are maturing, moving into mainstream
- FPGAs provide flexible way for leveraging productivity advantages of multi-core computing

# Call for Actions

- Please download Nios II Embedded Processor
  - http://www.altera.com/download
- Please visit SOPC World Booth for Demos



SOPC WORLD


Thank You
Q & A
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