# Understand and Design for High-Speed Memory Interfaces

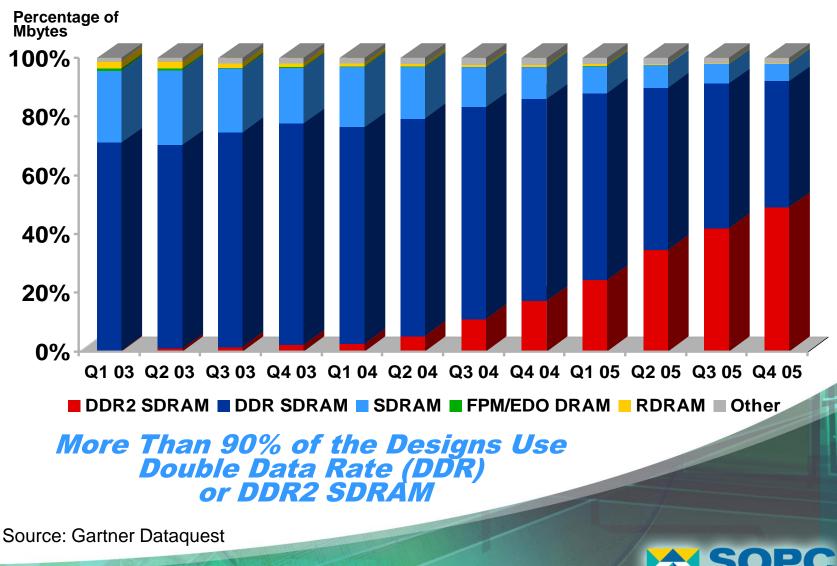


# Agenda

- Introduction
- Design challenges
- Overcoming design challenges
- Conclusion

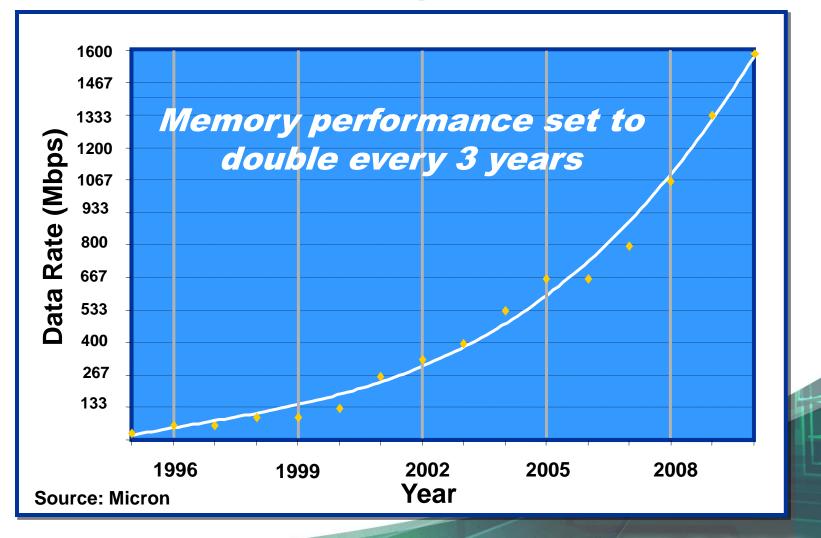


# **DRAM Quarterly Supply Trend**



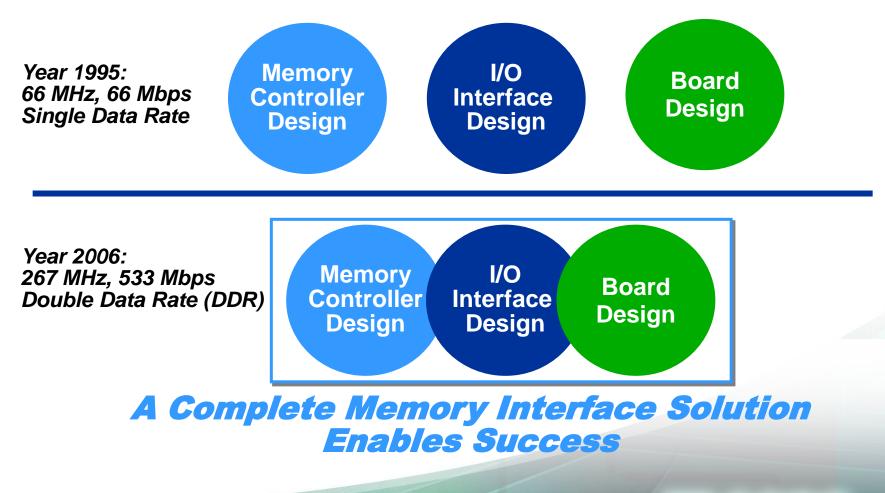
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## **Mainstream Memory Trends**





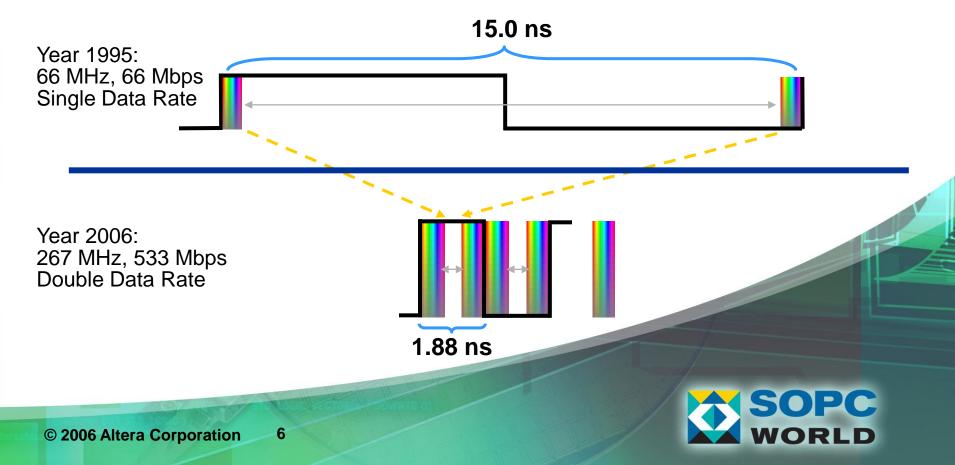
### Memory System Design: No Longer Separate Tasks





# Why a Dynamic System?

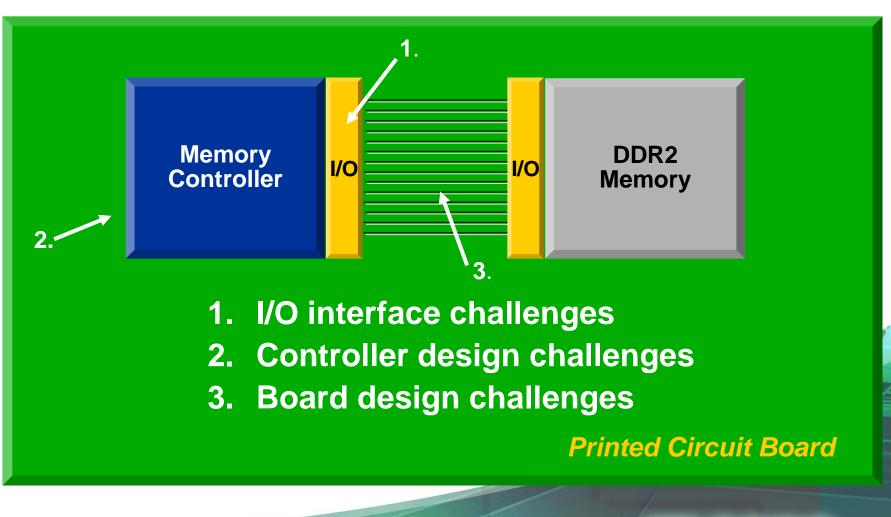
- Memory & board uncertainties do not scale with frequency
- Effects designers could once ignore are now significant proportions of the cycle



# **Design Challenges**



# **DDR2-533 Interface Design Challenges**





# **DDR2-533 Interface Design Challenges**

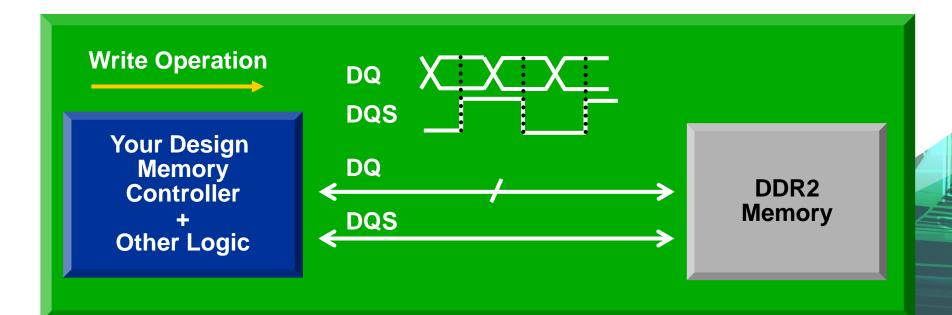
Challenges	Details
I/O interface	1. Maintaining DQ – DQS phase relationship
	2. Analyzing timing margin and meeting time requirements at the controller and memory I/Os
Controller design	<ul><li>1.Designing memory controllers</li><li>2.Verifying functionality</li><li>3.Managing clock domains</li></ul>
Board level	1. Maintaining signal integrity 2. Managing skew between signals



### I/O Interface Challenge #1: DQ-DQS Phase Relationship

#### Write Operation

- DQ and DQS to the memory are 90° apart
- Memory can easily capture write data

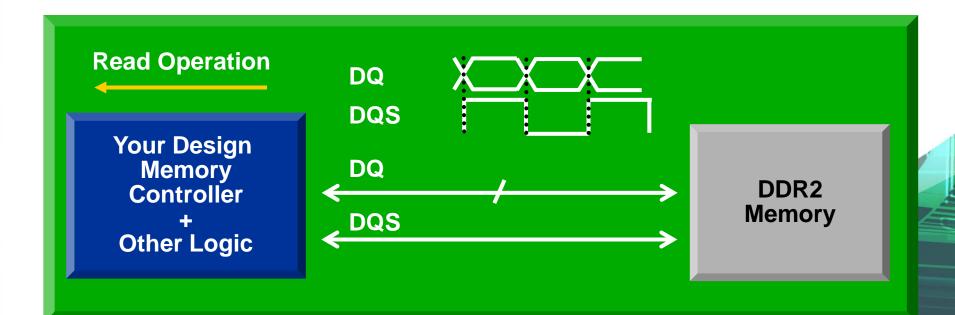




### I/O Interface Challenge #1: DQ-DQS Phase Relationship

#### Read Operation

- DQ and DQS signals from the memory are edge aligned
- DQS needs to be realigned to the center of data valid window





### I/O Interface Challenge #1: DQ-DQS Phase Relationship

Traditional techniques to realign DQS for read operation

Phase Shift Technique	Issues
90 <sup>0</sup> trace skew between DQ and DQS signals	<ul> <li>DQS signal is 6 inches longer than DQ signals*</li> <li>Complicated board design</li> </ul>
Add fixed delay element to the DQS signal path on board	Susceptible to process, voltage, and temperature (PVT) variations
Use on-chip delay elements	<ul> <li>Not suitable for high-performance applications</li> <li>Susceptible to PVT variations</li> </ul>

<sup>\*</sup> Calculation is based on approximate delay of 160 ps/inch for an FR4 laminate microstrip with a 50- $\Omega$  characteristic impedance at 533 Mbps data rate.



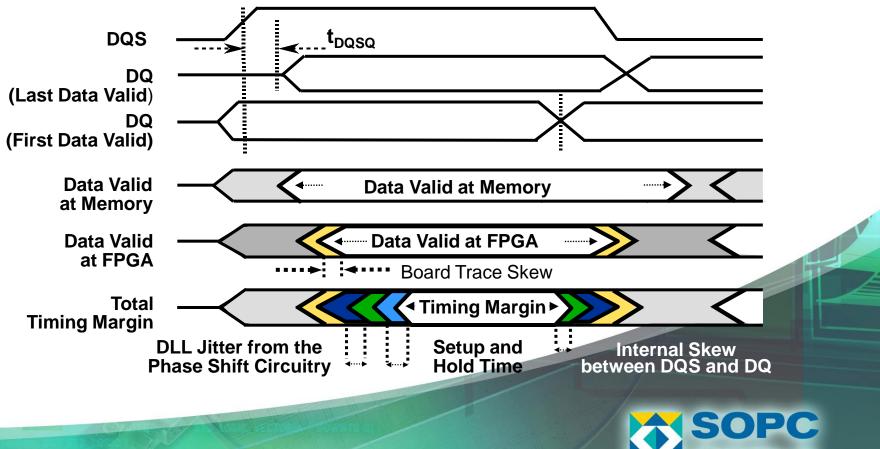
## I/O Interface Challenge #2: Timing Margin Analysis

- Parameters that affect timing margin
  - Skew between first data valid and last data valid
  - Board trace skew
  - DLL jitter for DQS phase shift circuitry
  - Internal skew between DQS and DQ
  - Setup and hold time



### I/O Interface Challenge #2: Timing Margin Analysis

 Timing margin = data valid window at memory - 2 x (board trace skew + DLL jitter + internal DQ and DQS skew) - setup and hold time



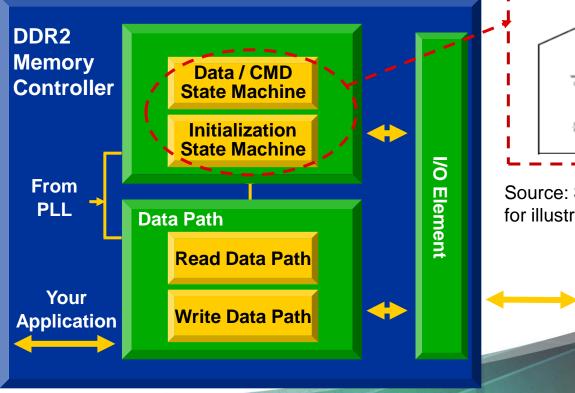
# **DDR2-533 Interface Design Challenges**

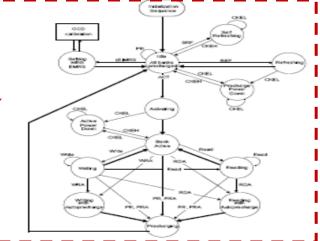
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Controller design	<ol> <li>Designing memory controllers</li> <li>Verifying functionality</li> </ol>
	3. Managing clock domains
Board level	1. Maintaining signal integrity 2. Managing skew between signals



# **Controller Design Challenge #1: Designing Memory Controller**

DDR2 memory controller block diagram





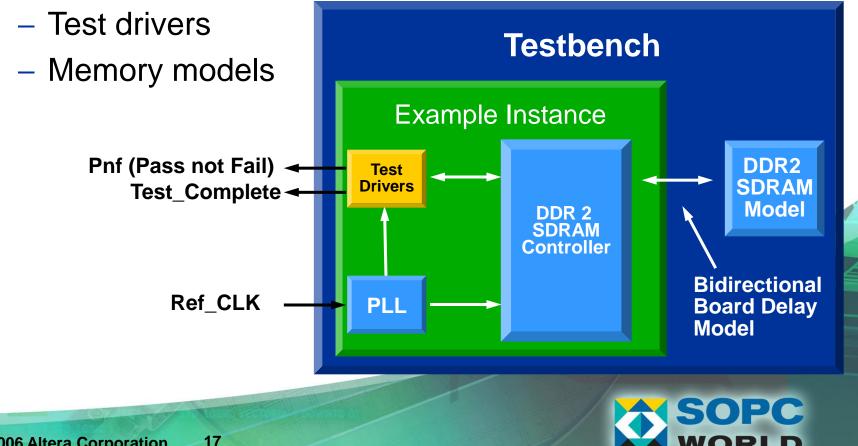
Source: Samsung. Simplified state diagram for illustration only.

DDR2 Memory



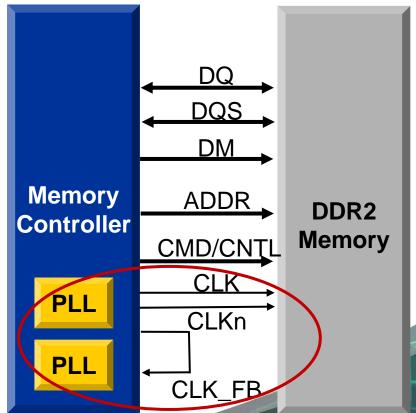
## **Controller Design Challenge #2: Verify Controller Functionality**

- Three major components in testbenches
  - Memory controller instance (unit under rest)



### **Controller Design Challenge #3: Clock Management**

- Resynchronization using clock feedback is essential for highspeed interface
  - Compensate PVT variations for I/Os
  - Achieve high-speed data rate (400 Mbps and above)





# **DDR2-533 Interface Design Challenges**

Challenges	Details
I/O interface	1. Maintaining DQ – DQS phase relationship
	2. Analyzing timing margin and meeting time requirements at the controller and memory I/Os
Controller design	<ul><li>1.Designing memory controllers</li><li>2.Verifying functionality</li><li>3.Managing clock domains</li></ul>
Board level	<ul><li>1. Maintaining signal integrity</li><li>2. Managing skew between signals</li></ul>



# **Board-Level Challenges**

Maintaining signal integrity

- Selecting right termination scheme
- Minimizing noise and signal crosstalk
- Minimizing signal attenuation
- Managing skew between signals
  - Making signal traces equal length



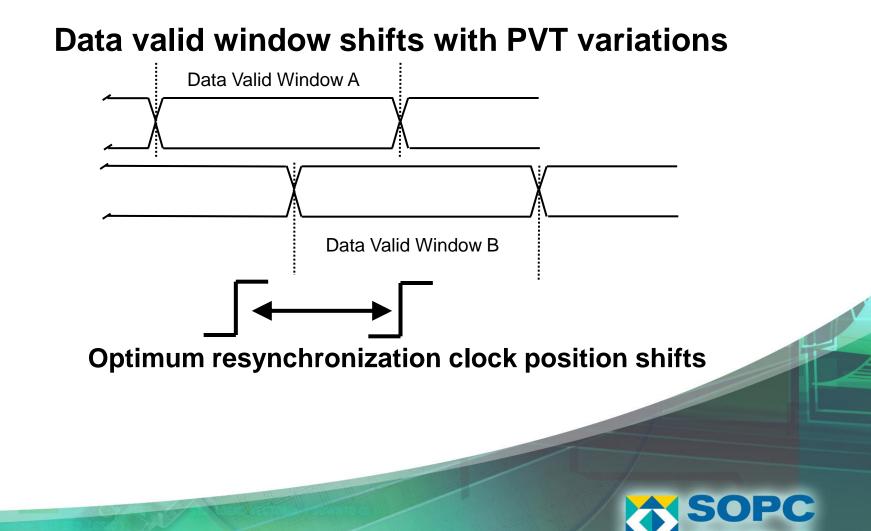
# **Factors Affecting Signal Integrity**

Design Item	Effect on Performance/Reliability of the System
Data width	Increasing data width increases simultaneously switching output (SSO) noise and increases board design complexity
Noise	Causes bit errors, affects signal integrity, and degrades performance and reliability
Loading	Increasing number of devices or modules will reduce performance
I/O performance	Drive strength affects quality of signals and maximum clock rate
Termination scheme	Termination scheme and resistor values affect signal quality and performance

Board Simulations Should Be Performed to Check for Signal Integrity

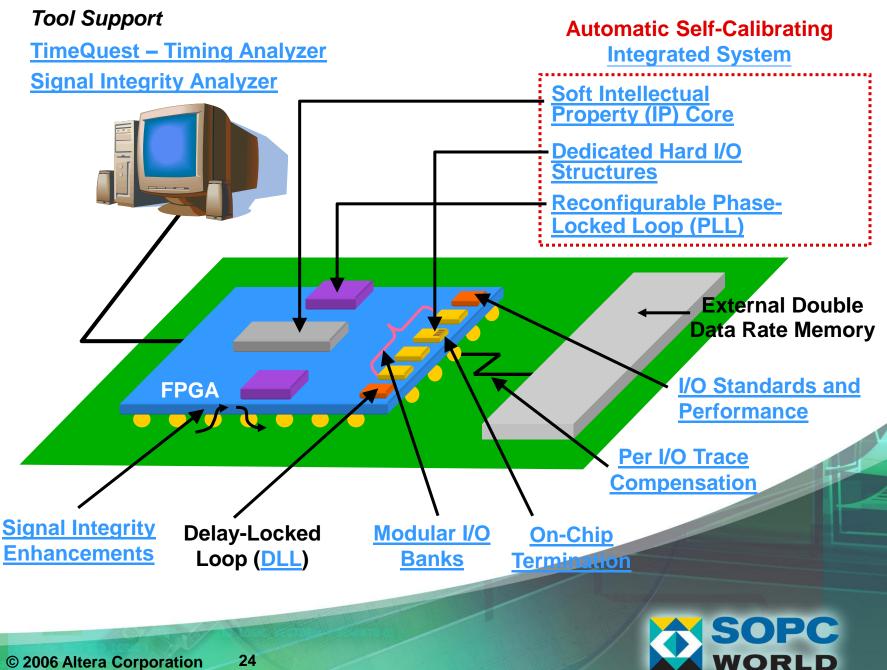


# **Data Valid Window Shifts**



# **Overcoming Design Challenges**





# **FPGA I/O Capabilities**

#### External memory interfaces support on all I/O banks

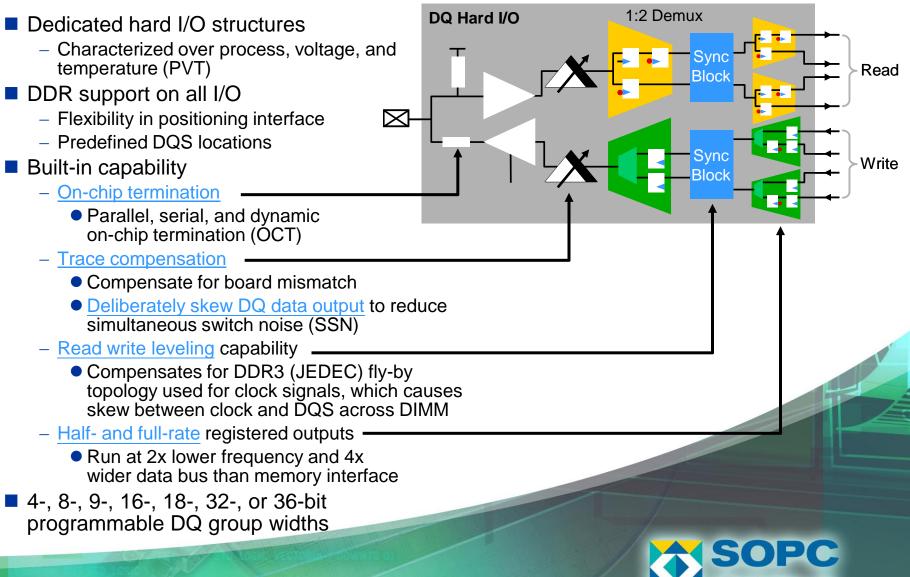
	Device Family			
Interconnect	Stratix <sup>®</sup> III	Stratix II		
	Performance*	Performance		
DDR III	400 MHz	N/A		
DDR II	400 MHz	333 MHz		
DDR	200 MHz	200 MHz		
QDR II	350 MHz	300 MHz		
QDR II+	400 MHz	N/A		
RLDRAM II	400 MHz	300 MHz		

\*Stratix III left and right banks support 300-MHz DDR rates.

Memory Interface Standard	I/O Standard
DDR III	1.5-V SSTL-1.5
DDR II	1.8-V SSTL-1.8
DDR	2.5-V SSTL-2
QDR II	1.8-V HSTL
QDR II+	1.5-V HSTL
RLDRAM II	1.8-V HSTL



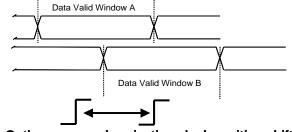
# **Specialized I/O Structures**



# **Meeting Timing Margins**

- Used to maintain best setup and hold margins
  - Voltage and temperature variations cause data valid window to shift
  - Shifting resynchronization clock edge by same amount maintains best setup and hold margins
  - Free soft IP core monitors voltage and temperature variations and automatically adjusts resynchronization clock phase
- One PLL drives all clock signals required for interface
  - Stratix III PLLs have 7 to 10 outputs
  - DDR uses 3 to 7 clocks; QDR uses 4 to 5 clocks
  - Only 1 PLL required per interface
    - 2 required for >200 MHz in Stratix II devices
- No interruption of external memory interface operation when PLL reconfigured

#### Data valid window shifts with PVT variations



Optimum resynchronisation clock position shifts

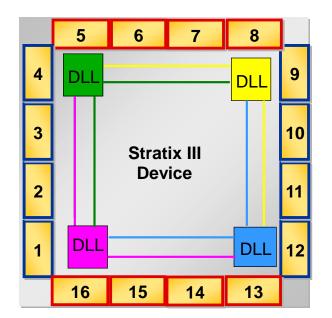


# **Maintaining Phase Shift Relations**

DLL dynamically adjusts DQS delay chain to maintain phase shift over PVT

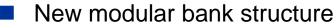
### 4 DLLs

- Each has 2 independent outputs
- Each I/O bank can access 2 DLLs
- Allows external memory interfaces with different frequencies and phase shifts to coexist on same side





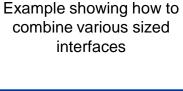
# **Efficient Modular I/O Banks**

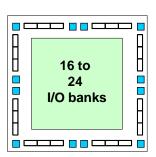


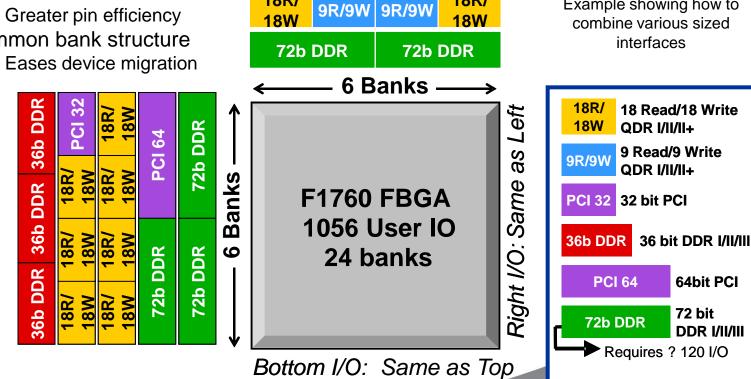
- Many small I/O banks
  - Fixed bank widths: 24, 32, 36, 40, or 48 user I/Os per bank

18R/

- 16 to 24 banks
- Greater pin efficiency
- Common bank structure
  - Eases device migration





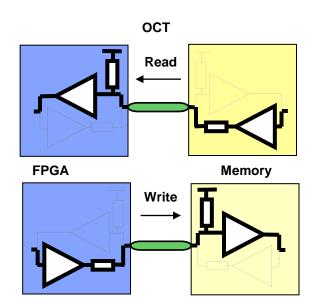


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# **On-Chip Termination on All Banks**

- Parallel serial and dynamic on-chip termination for single ended DQ pins
- Dynamic termination for better control of reflections
  - Writes
    - Series termination enabled
    - Parallel termination disabled
  - Reads
    - Series disabled
    - Parallel termination enabled
- Calibrated for repeatable and predictable termination
  - Tolerance controlled with digital auto calibration circuits

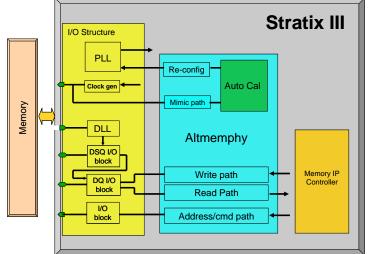




### **Integrated System for Rapid Implementation**

### Altera offers free ALTMEMPHY megafunction to maximize performance

- ALTera external MEMory PHYsical layer interface
- Integrates hard I/O blocks and soft logic data path section
- Self-calibrating
- Optimized to take advantage of Stratix III silicon features
- Simple user interface
- Complexity kept inside





### Self-Calibrating for Highest Reliable Frequency of Operation Across PVT

### Self-calibrating control block

- Training pattern
  - Calibrates out process differences on both FPGA and external memory
  - Works on a pin-by-pin basis
- Monitor and Adjust
  - Monitors voltage and temperature variations during operation via mimic path
  - Adjust resynchronization phase of PLL output without interrupting operation

External Memory Device Initialisation (performed by the memory controller)	Write data training	Calibration	Functional use of the memory	



# **Configurable Megafunction**

- Quickly and easily configure physical layer interface to match desired memory
- Optimized to take advantage of Stratix III I/O structures and hard blocks
- Constrained with Synopsys design constraints (SDC)
  - Industry standard
  - Easy to constrain data with respect to sourced clock

ettings	Summary Page				
iab3 1	ab2 Tab1				
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Memory type		-			
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	ce clock frequency	-	MHz (2500 ps)		
PLL phase s			steps		
Memory PH		-			
Speed grade	2	-			
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		P	roperty	Value	Units
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	T46V16M8TG-6T T46V8M16TG-75				
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# **TimeQuest Timing Analysis Tool**

#### ASIC strength timing analysis tool

- Native support for industry-standard SDC timing constraints
- Easily constrain source synchronous interface
  - Constrain data with respect to clock

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-B Summary	1 From Node state_mcinot18iter.tap4	Type (Delay (ps))	2 Quartus II Static Timing Analyzer Tool - D:/q60/quartus/designs/chiptrip/chiptrip_cycloneii/chiptrip 💷 🔀
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	3 Launch Clock clk	Cel (4740) (48%)	Popot * Data not available
	4 Latch Clock dk		Report
	5 Date Anival Time 12.165		- W Messages (Not wedring yet) Report: Timing
	6 Data Required Time 12.233 7 Slack 0.068		- CS Summary Enter values to recent limiting outful. All values are optional Clicking the Record
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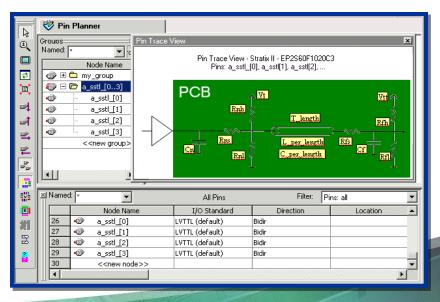
# **Robust Signal Integrity Tool Support**

### Quartus II signal integrity analyzer

 Drives signal integrity analysis and automatic optimization

### Signal integrity advisor

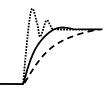
Provides design-specific guidance





# **Per I/O Trace Compensation**

- Programmable single-ended I/O features that help compensate for trace characteristics
  - Controllable slew rate
    - 4 settings to match desired I/O standard and control noise and overshoot
  - Programmable output drive strength
    - Match desired I/O standard
  - Programmable output delay
    - Board trace mismatch compensation
    - Deliberately skew DQ data output
      - Reduce simultaneous switching noise (SSN)



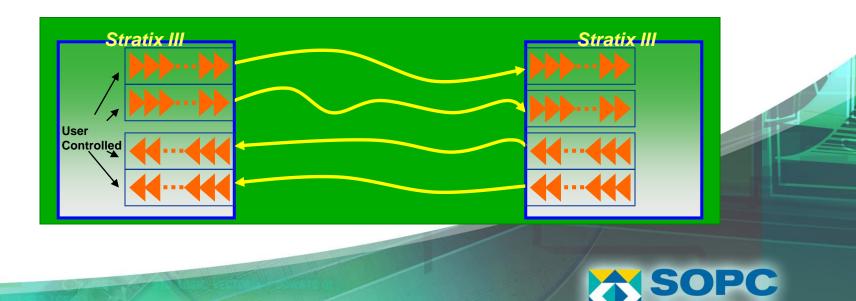
#### Settings depend on standard, SSTL-18 example shown

I/O Standard	mA	mA	mA	mA	mA	mA
SSTL-18 Class I	4	6	8	10	12	
SSTL-18 Class II			8			16



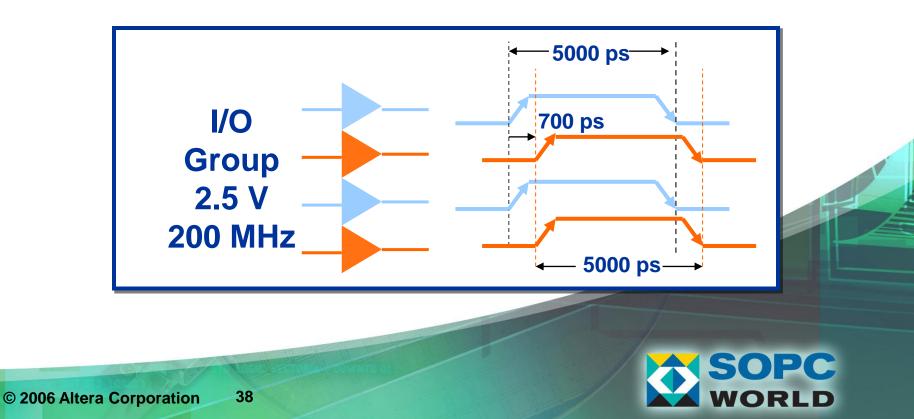
### **Board Trace Mismatch Compensation**

- Output delay per I/O: 0 to 1000 ps
- Input delay per I/O: 0 to 800 ps
- Digitally programmable in 50 ps steps
- Compensation for 0 to 5 ½ inches
  - FR4 delay: ~170 ps/inch



### **Deliberately Skew DQ Data Output**

- Reduce SSN
  - Delaying adjacent edges reduces total number of simultaneous switching output (SSO) edges
  - Controllable in 50 ps steps



# **Signal Integrity Enhancements**

- Programmable slew rate
  - Lowering signal rise time reduces ∂i/∂t
- Signal integrity die and package enhancements
  - Increased number of power/ground pairs reduces L
  - Deliberately skew DQ data output
    - Delaying adjacent edges to reduce simultaneous edges

SSN Depends on Loop Inductance and Signal Rise Time L ∂i/∂t



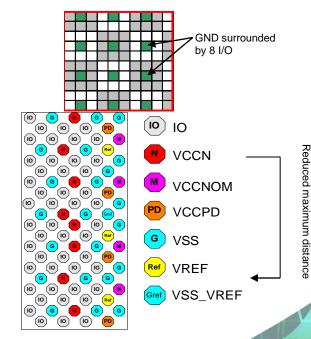
# Signal Integrity Package and Die Enhancements

#### Package enhancements

- 8:1:1 user I/O-ground-power ratio
- Limited number of I/Os per bank
- Maximum distance between I/O and GND = 1
  - Reduced loop inductance in package

#### Die enhancement

- Extensive distributed ground bumps
  - Enhanced return path
- Programmable edge rate control
- Programmable staggered outputs
  - Control SSO noise

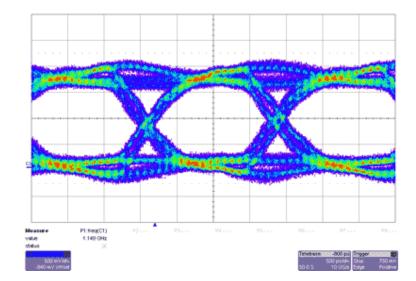




### 667-Mbps DDR2 SDRAM Interface



#### DDR2 SDRAM Write Data Eye 667 Mbps



#### \*For Stratix II Devices



# Conclusion

- Interfacing with external memory devices has I/O timing, controller design, and board design challenges
- Stratix series FPGAs from Altera provide advanced features to meet I/O interface challenges
- Fully verified hardware platforms including Altera IP and board design tools simplify memory interface design



# Thank You Q & A

