SOPC WORLD 2004

Ensuring Success in High-Speed System Design

ALTERA®

Today's-High Speed Systems

- High-Speed Designs Require Faster Devices & Increasing Data Widths
- Wide Data Buses Demand Higher I/O Pin Count
- Faster Devices Exhibit Faster Edge Rates
- A Memory Interface is a Typical Example for Such a System

Agenda

- Memory Interface Design
- Simultaneously Switching Outputs
- Altera Design Resources
- References

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Memory Interface Design

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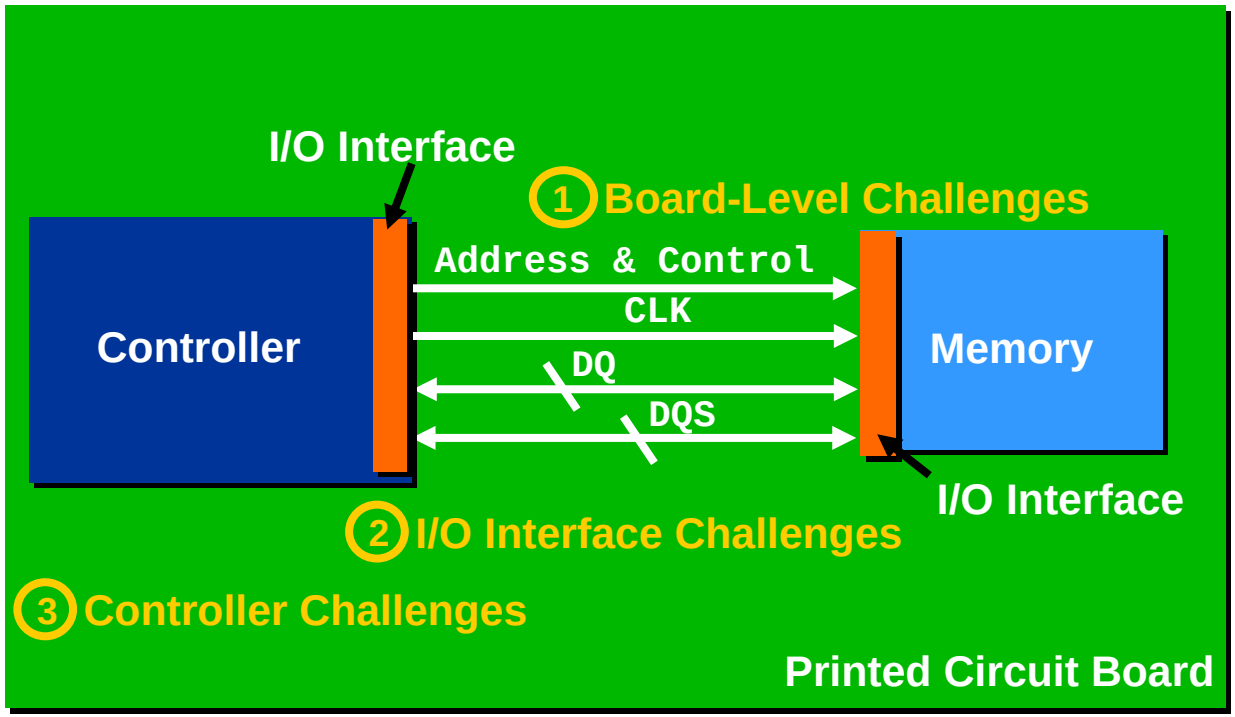
Memory Interface Design Challenges

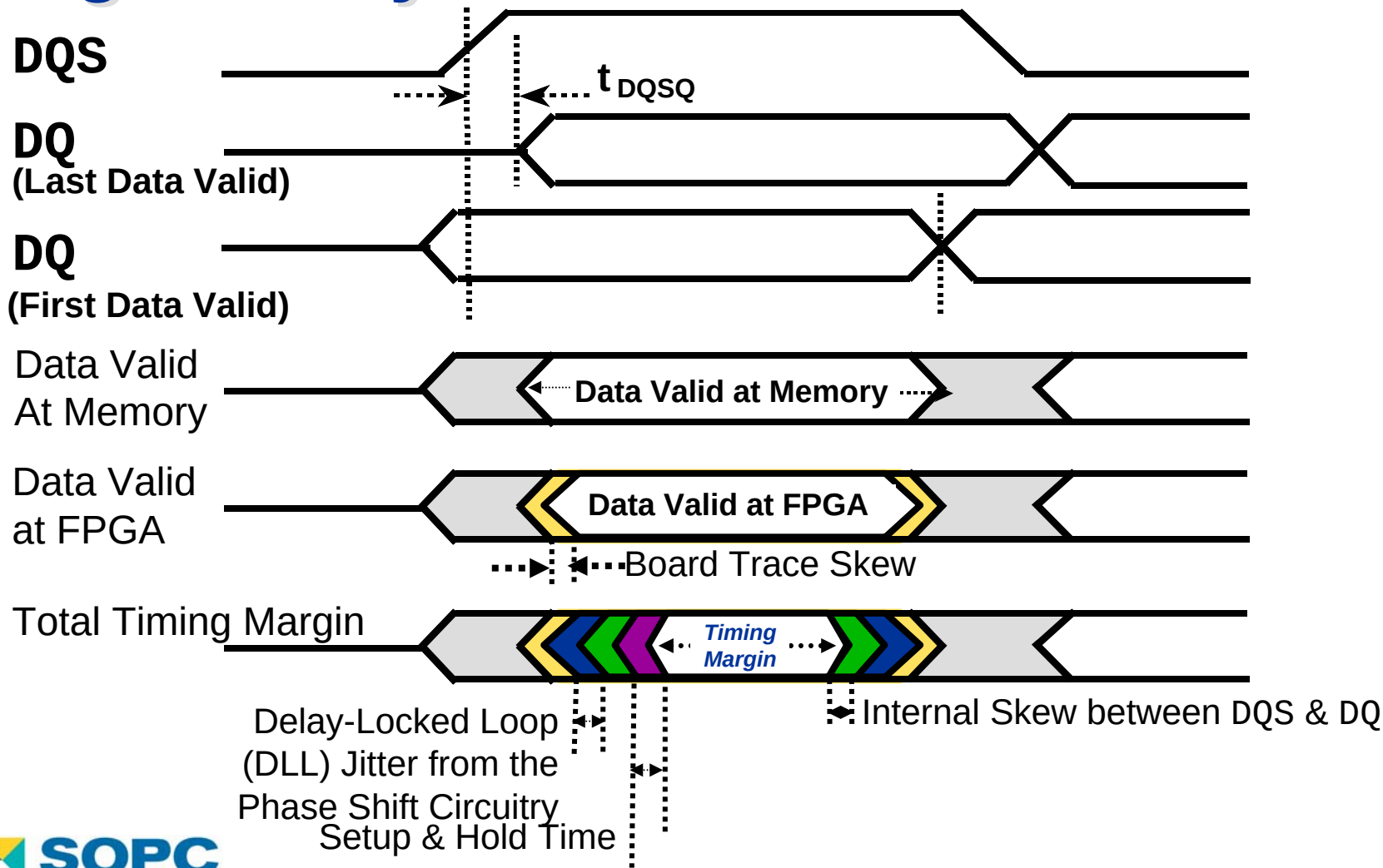


The Higher the Frequency, the Greater the Design Challenge

Altera Memory Interface Solutions

Challenge	Altera Resolution
Board-Level Challenges	■ Simultaneous Switching Outputs (SSO) Guidelines ■ Fully Verified Hardware Reference Platforms with Gerber Files ■ Termination Recommendations & Board Design Guidelines ■ SPICE & IBIS I/O Simulation Models
I/O Interface Challenges	■ DQS Phase Shift Circuitry in Stratix® Series FPGAs ■ Detailed Timing Margin Analysis for Non-IP Users ■ Fully Optimized Memory Controller Intellectual Property (IP) Cores with Automatic Timing Analysis for IP Users
Controller Design Challenges	■ Fully Optimized Memory Controller IP Cores with Automatic Timing Analysis & Functional Simulation Capabilities ■ Feature-Rich Phase-Locked Loops (PLLs) to Manage Clocks

Example: DDR2 Read Timing Margin Analysis



Signal Integrity & Board Design

Design Item	Effect on Performance/Reliability of the System
Bus Width	Increasing Bus Width Increases SSO Noise & also Increases Board Design Complexity
Noise	Causes Bit Errors, Effects Signal Integrity & Degrades Performance & Reliability
Loading	Increasing Number of Devices or Modules will Reduce Performance
Termination Scheme	Termination Scheme & Resistor Values Affect Signal Quality & Performance

Board Simulations Should be Performed to Check for Signal Integrity

Simultaneously Switching Outputs

- Increased Bus Width, Pin I/O Counts & Inherent Package Trade-Offs Can Introduce More SSO Noise
  - I/O Count vs. I/O Drive Strength
- An FPGA Offers the Flexibility to Employ Reduction Techniques to Minimize Detrimental Effects of SSO

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Simultaneous Switching Outputs (SSO)

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Components of SSO Noise

- Ground Bounce
- Power Bounce Commonly Referred to as Vcc Sag

What is SSO Noise?

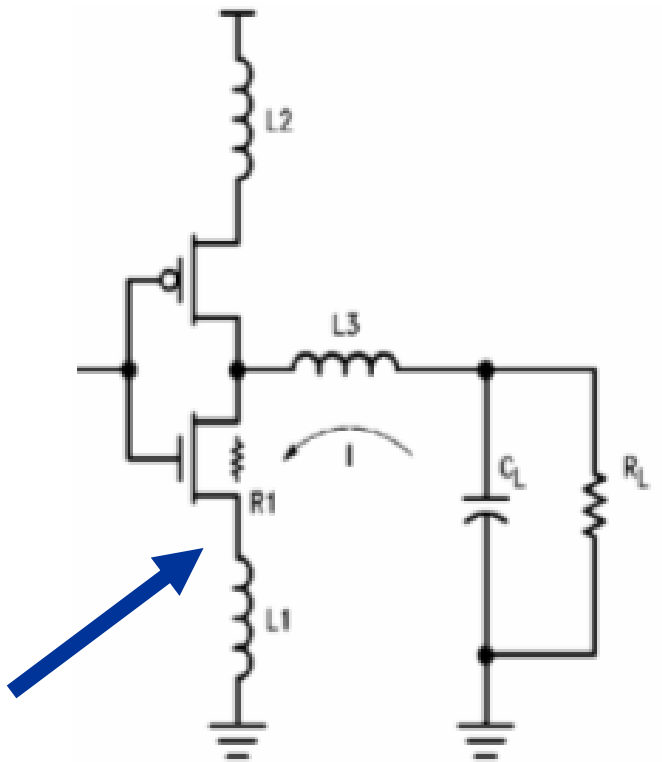
- Ground Bounce & Vcc Sag are Voltage Fluctuations on a Static Signal (Quiet) as a Result of High Current Change (di/dt) from Nearby I/O Buffer Circuitry that Share Common Ground (Vcc) Return Paths
- Ground Bounce Affects Static Low Signals;
  Vcc Sag Affects Static High Signals
- Enough Ground Bounce or Vcc Sag on a Static Signal May Cause Sampling of Wrong Data, Depending on:
  - I/O Standard Used
  - Available Noise Margin
  - Amount of Ground Bounce
  - When the Signal is Sampled

Ground Bounce Circuit Model

- L1 is Lumped Inductance for Die, Bump, Package, & Ball
- Output Buffer Current

  $i(t) = C * dv/dt$
- Voltage Across L1

  $v(t) = L * di/dt$
- High-to-Low Transitions on Output Raises Local Ground V



Ground Bounce Circuit Model

- Key Equations

  $i(t) = C * dv/dt$

  $v(t) = L * di/dt$

- Output Voltage (b) with Certain Slew Rate
- Induces Current (c) through Pull-Down Transistor & L1
  - Ideal Waveform
- Creates Voltage Ground Bounce (d) in Local Ground, through Other Quiet Low Outputs via NMOS Transistors

b. Output Voltage (V)

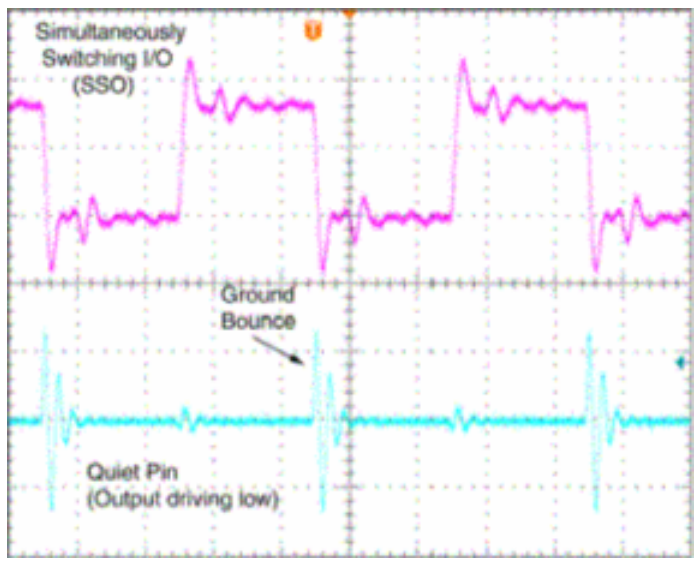
c. $I = -C_L \bullet (\Delta V/\Delta t)$

d. $V_{GB} = L \bullet (\Delta I/\Delta t)$

Impact of Ground Bounce (cont.)

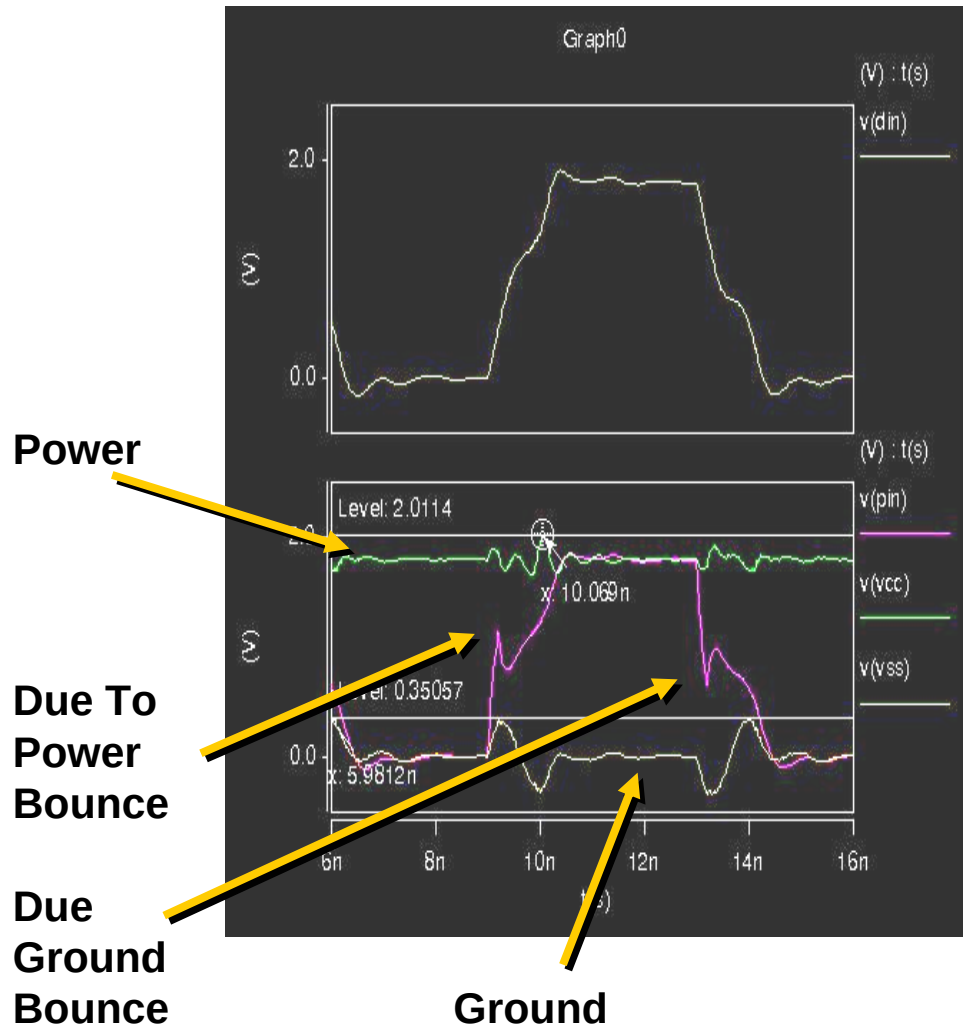
- If Enough Outputs Switch Simultaneously to Induce 0.8V of Ground Bounce on a Nearby "Victim" Pin, that Pin Momentarily Glitches to 0.8V
  - 3.3-V LVTTL, Maximum V_{IL} is 0.7V

- If Victim Pin is Clocked During the SSO Event, the Sampled Value May Be Wrong
  - Similarly Applies to Vcc Sag & V_{IH} Minimum.



Impact of Ground Bounce

- Ground Bounce
  - Effects Worse than Power Bounce
  - Can Cause Logic 1 Instead of 0 in Extreme Cases
- Vcc Sag
  - Causes Drop in Power Supply
  - Can Affect Outputs
- Both Cause Degradation in Waveforms



Elements That Contribute To SSO Noise

- Package:
  - Number of Power/Ground Pins
  - Reference Planes
  - Decoupling
  - Package Type (Flip-Chip vs. Wirebond)
    - Majority of SSO Noise Occurs at Package Level
- Board:
  - Decoupling Capacitors
  - Power Ground Planes
  - Sockets
  - Vias

Packaging

- Wire-Bond: Lacks Referencing Structures for Every Signal Trace, thus Contributes to Overall High Inductance
- Flip-Chip: Signal Bumps Enter the Package Laminate without Having to Traverse through Long, Unreferenced Wire-Bonds

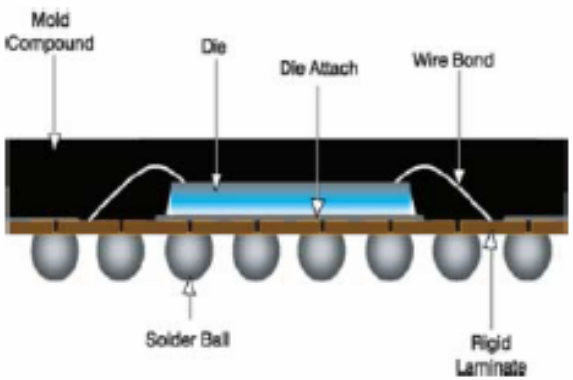


Figure 1.6 – Wire bond package cross section

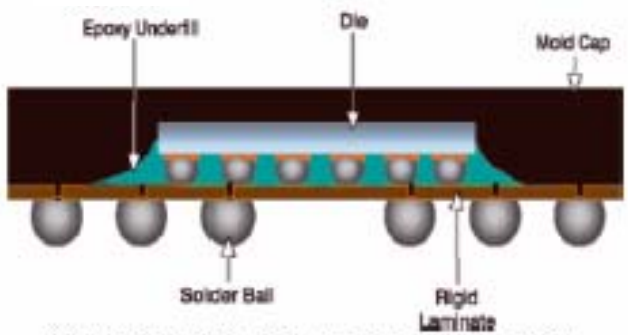
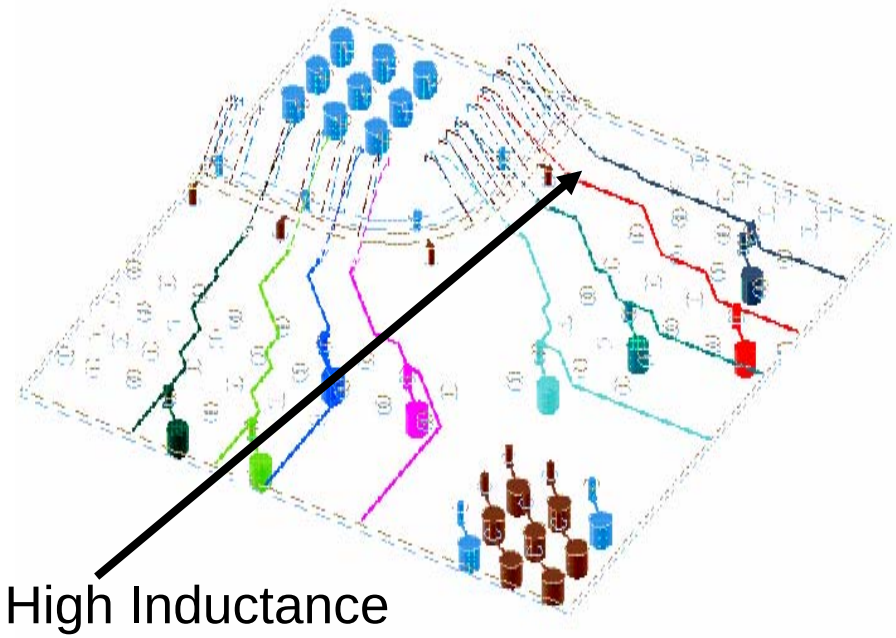


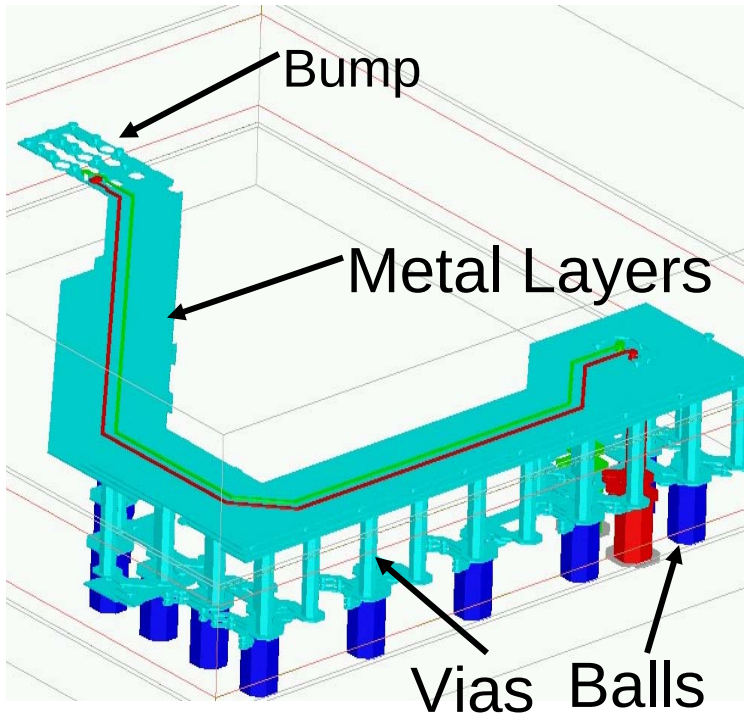
Figure 1.7 – Flip Chip package cross section

Packaging

Flip-Chip Vs. Wire-Bond



Wire-Bond



Flip-Chip

Techniques For Reducing SSO Noise

- Use Flip-Chip Package
- Add/Utilize Better Return Paths
  - Use Unused I/O Pins as Programmable Vcc & GND
- Use Lower Drive Strength
- Use Slow Slew Rate (SSR) vs. Fast Slew Rate (FSR)
- Proper I/O Pin Selection
- Add Decoupling Capacitors & on Board Power Ground Capacitance
- Proper Trace Layout
- Remove Sockets
- Use On-Chip Termination

All Techniques Verified Using Stratix® & Stratix GX Reference Boards

Utilize Unused I/O Pins as Programmable Vcc & GND

# of I/O Pins Switching	Ground Bounce (mV)	Vcc Sag (mV)
20: All Pins Switching	650	1,020
20: Every Other I/O Pin switching	490	910
20: Every Other I/O Pin Switching & Every Other Tied to Ground	364	820
20: Every Other I/O Pin Switching & Every Other Tied to Power	490	700
24: Every Third I/O Pin Switching, Every Third Tied to Power & Every Third Tied to Ground	300	320

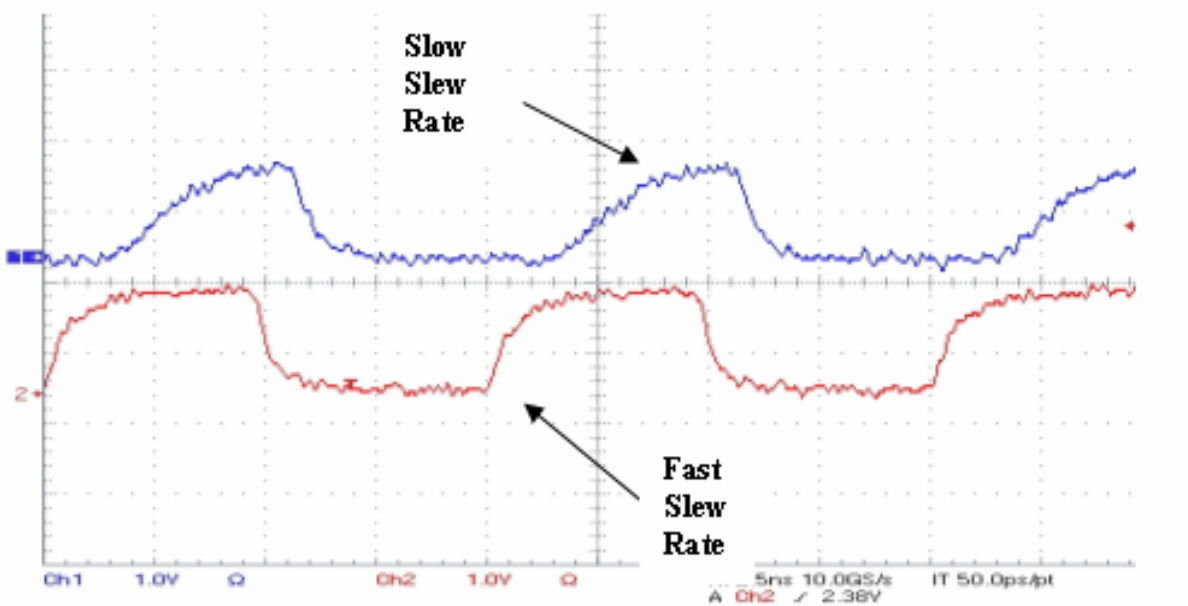
Results For 24 mA LVTTL I/O Pins

Use Lower Drive Strength

# of I/O Pins Switching	Drive Strength	Ground Bounce (mV)	Vcc Sag (mV)
20: All I/O Pins Switching	24 mA	650	1,020
20: All I/O Pins Switching	12 mA	456	730
20: All I/O Pins Switching	4 mA	328	660

Results For LVTTL I/O Pins

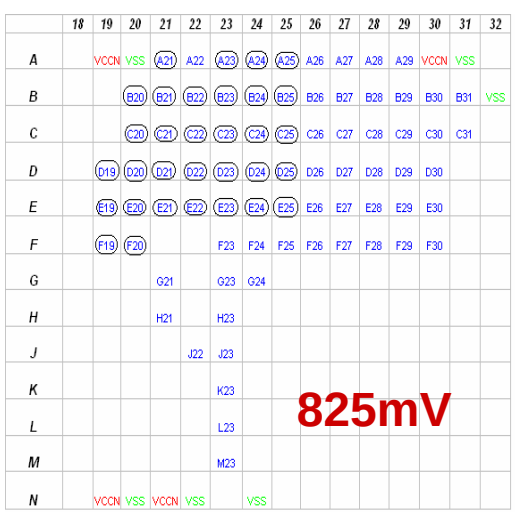
Turn on Slow Slew

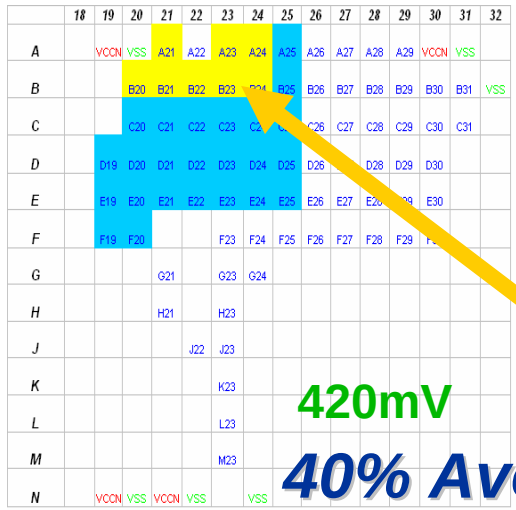


8 mA Drive Strength, 40 3.3-V LVTTL I/O Pins, Switching Simultaneously

Switching	With Fast Slew Rate	With Slow Slew Rate
Bounce (mV)	288	200
Vcc Sag (mV)	620	310

Delay Shift SSO pins



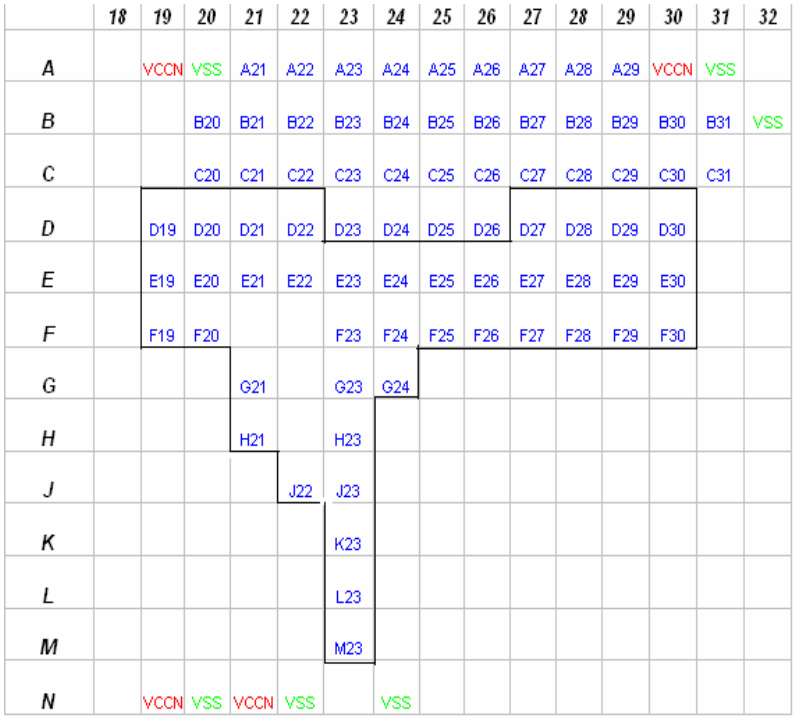


32 SSO, w/ 8 pins delayed by 3ns (in yellow)

40% Average Reduction!

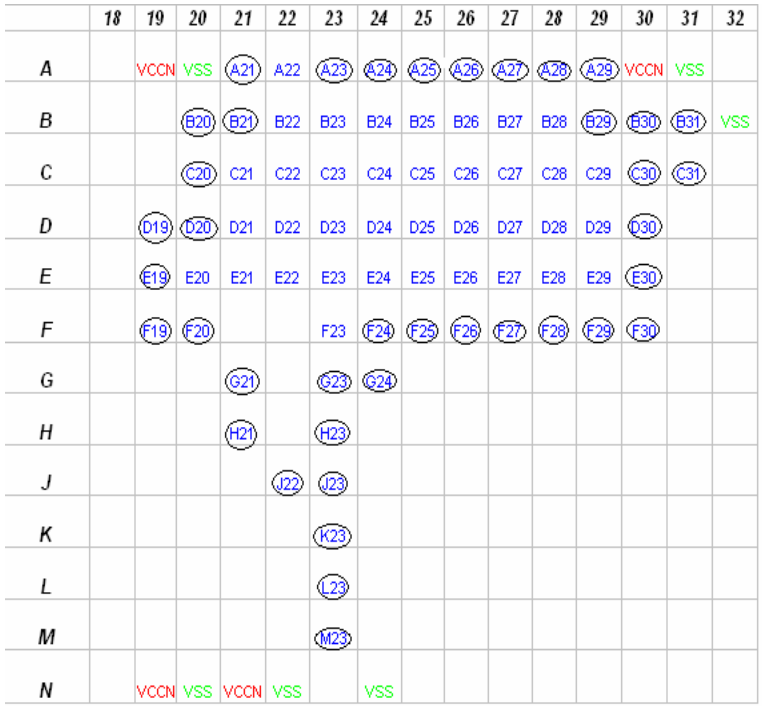
- Reduces Current Density
- Add PLL Phase Shift, or Add Output Timing Delays

Spread Out Selected I/O Pins



	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

Bounce = 570
Sag = 1,017 mV



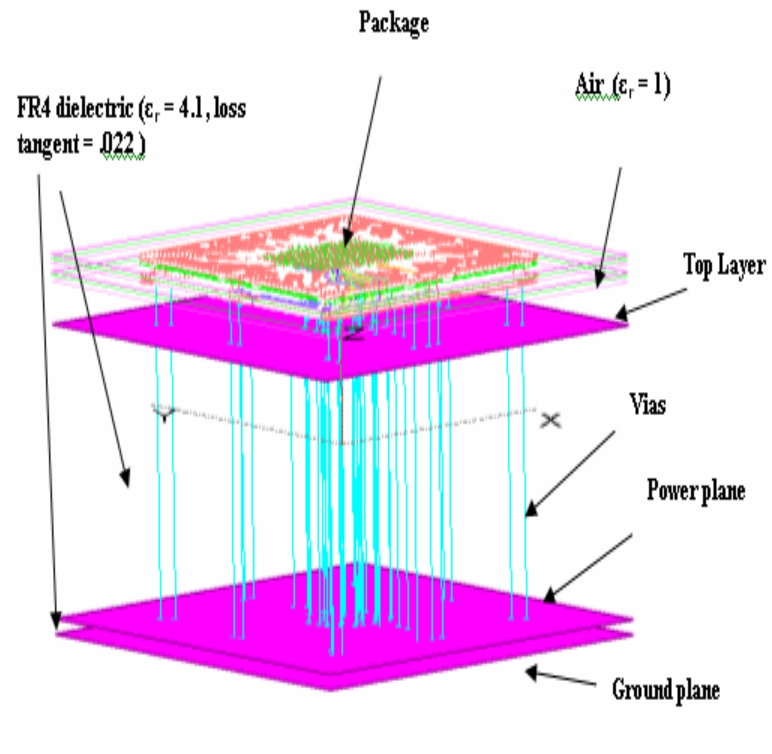
	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

Bounce = 412
Sag = 810 mV

On-Board Power Ground Capacitance

- Solid Power & Ground Planes

Configuration	Ground Bounce
Ground/Power, 140 mils from IC, 6 mils Apart	370 mV
Ground/Power, 20 mils from IC, 6 mils Apart	248 mV
Ground/Power, 20 mils from IC, 4 mils Apart	228 mV



Decoupling Capacitors

- Decoupling Capacitors Provide Localized Power Supply
  - Capacitance Stores Energy & Provides It When There Is Transient Requirement
- When Solid Power/Ground Sandwich Present, High Frequency on Board Capacitors Can Be Useless if Path to IC Is Very Inductive
- Bigger Capacitors Are Effective for Lower Frequency Noise

Stratix II FPGAs Offer On-Chip Decoupling, an Optimal Solution to Provide Better Return Paths

Other Techniques

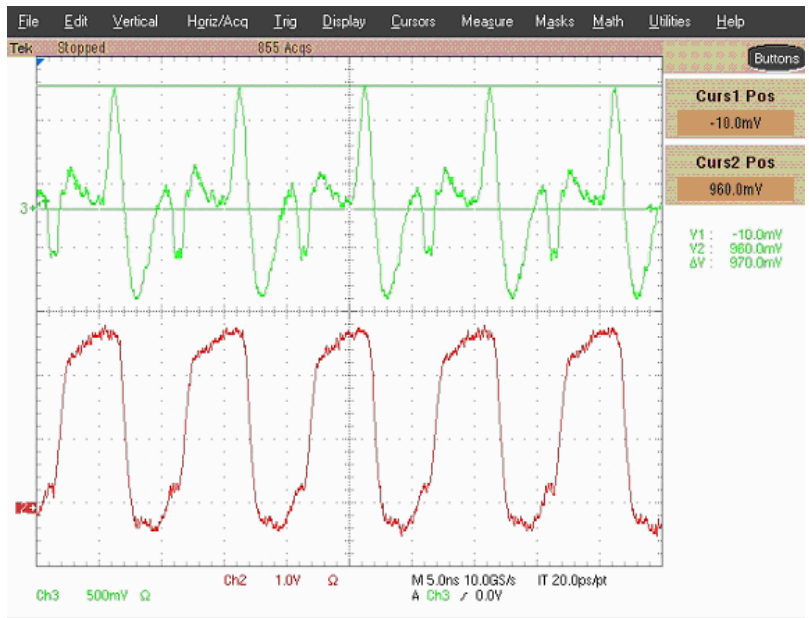
- Don’t Use Any Sockets between IC & Board
  - Reduces Inductance
- Differential Signaling Helps with SSO
  - Traces Should Be Tightly Coupled
- Series On-Chip Termination Reduces SSO by Absorbing Reflections
  - Slows Edge Rate

Worst Case (Before Optimization)

- Combination of Several Factors Can Significantly Reduce Ground Bounce & Vcc Sag Noise

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

970mV



40 SSO Pins, 24-mA Current Drive, FSR, No Delay, No Programmable Grounds

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Nominal Case

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

430mV

40 SSO Pins, 36 Interleaved Programmable Powers (Red) & Grounds (Green), 16-mA Current Drive, FSR, 22 Pins with 3-ns Delay (Yellow)

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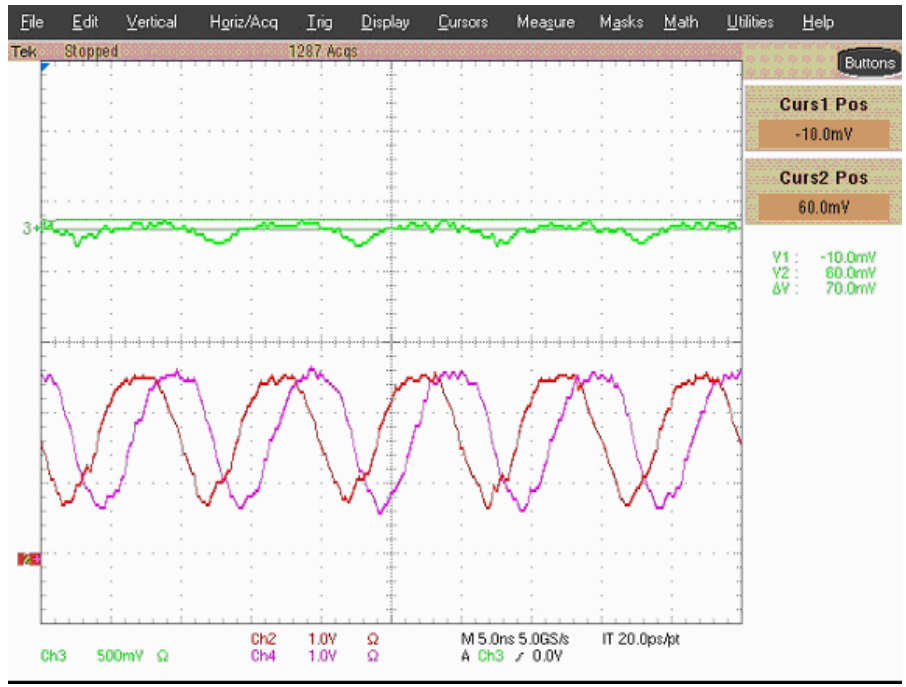
Best Case

	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
A		VCCN	VSS	A21	A22	A23	A24	A25	A26	A27	A28	A29	VCCN	VSS	
B			B20	B21	B22	B23	B24	B25	B26	B27	B28	B29	B30	B31	VSS
C			C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	
D		D19	D20	D21	D22	D23	D24	D25	D26	D27	D28	D29	D30		
E		E19	E20	E21	E22	E23	E24	E25	E26	E27	E28	E29	E30		
F		F19	F20			F23	F24	F25	F26	F27	F28	F29	F30		
G				G21		G23	G24								
H				H21		H23									
J					J22	J23									
K						K23									
L						L23									
M						M23									
N		VCCN	VSS	VCCN	VSS		VSS								

70mV!



40 SSO Pins Far Away, 36 Programmable Powers (Red) & Grounds (Green) around Quiet Pin, 4-mA Current Drive, SSR, 20 Pins with 3-ns Delay

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Altera Design Resources

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Modeling

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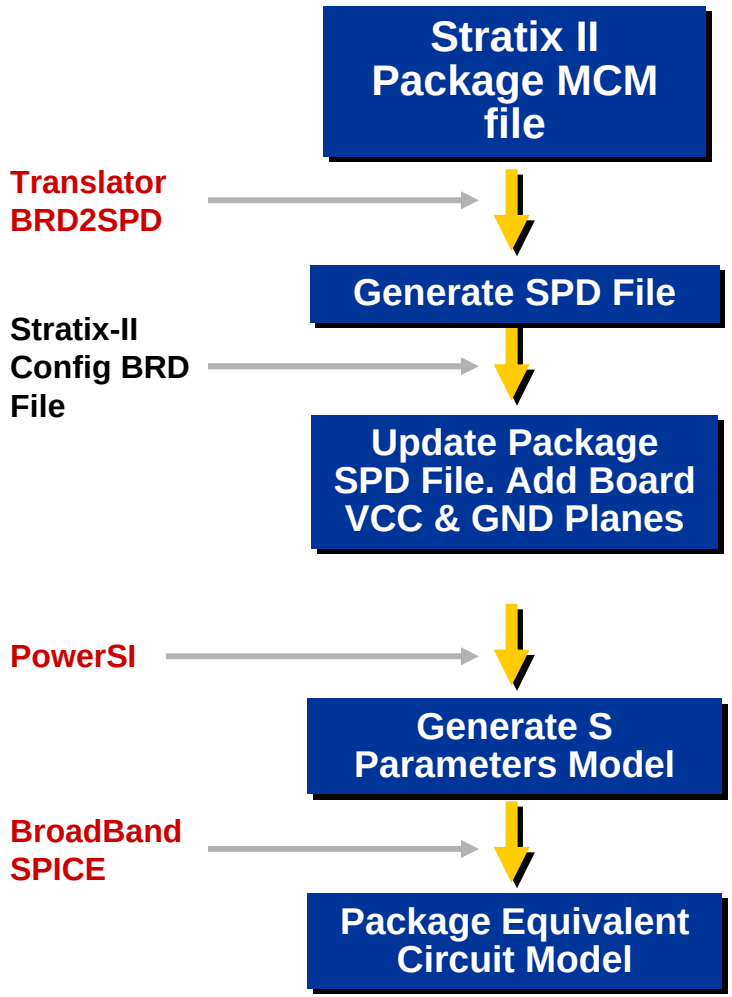
Objective of SSO Modeling

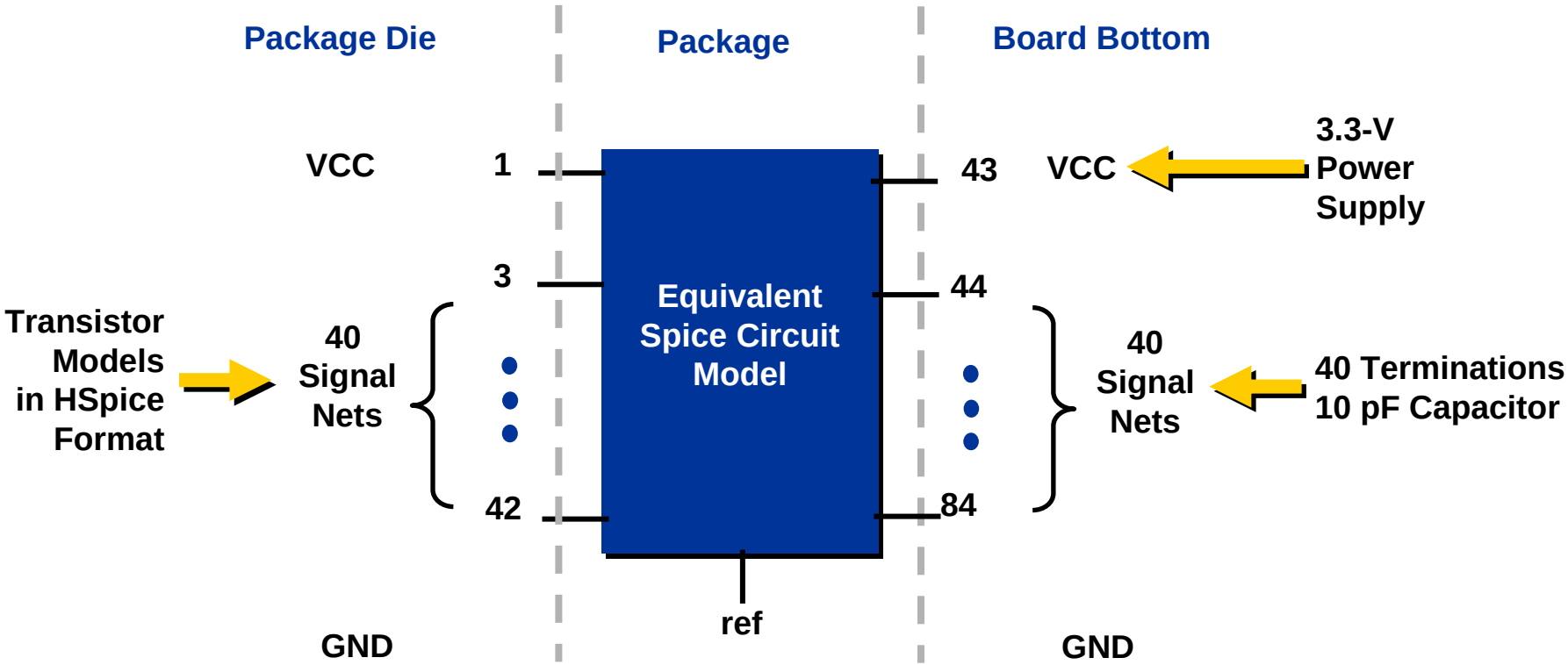
- Explore, Derive & Verify a Robust Methodology that Can Be Consistently Used in Future SSO Analysis
- Simulate & Correlate the Results Obtained from Lab Measurements
- Generate & Validate Simulation Models that Can Be Used as a Black Box for ‘what-if’ Analysis

SSO Model Extraction Flow

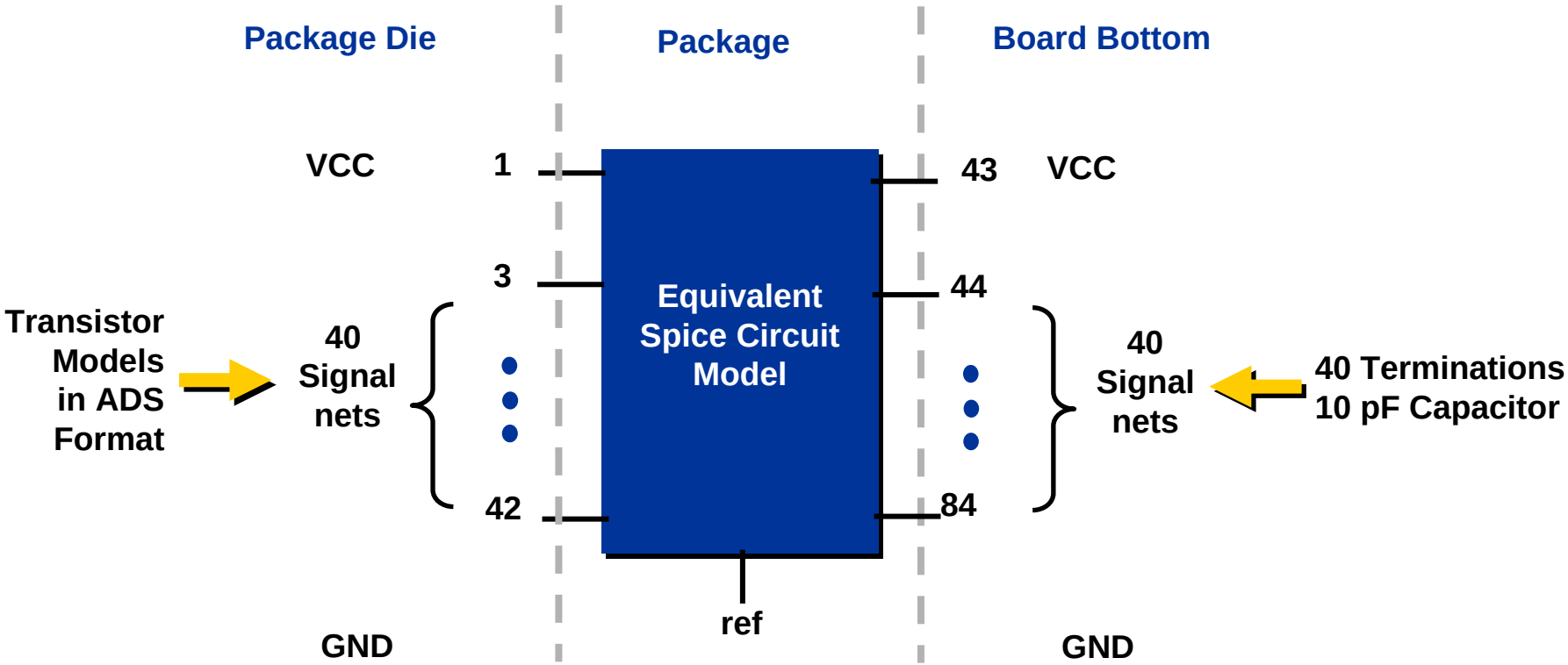
- Translation of Database
  - Translate Package MCM File into Sigrity SPD Format
- Structure Verifications/Modifications
  - Verify Stackup, Material Properties, Plane Shape, Via/Trace Dimensions
  - Add Board VCC & Ground Planes
  - Others
- Mesh Settings
  - Add Solder Ball Vias
- Error Corrections
- Coupled Line Selection
- Define Ports
- Pre-Simulations Tests
  - DC Test
  - AC Test
  - Signal Transmission Test



Simulation Flow Using HSpice



Simulation Flow Using ADS (Optional)



The Simulation Flow Will Be Updated after ADS Model Becomes Available.

SSO Modeling Matrix Chart

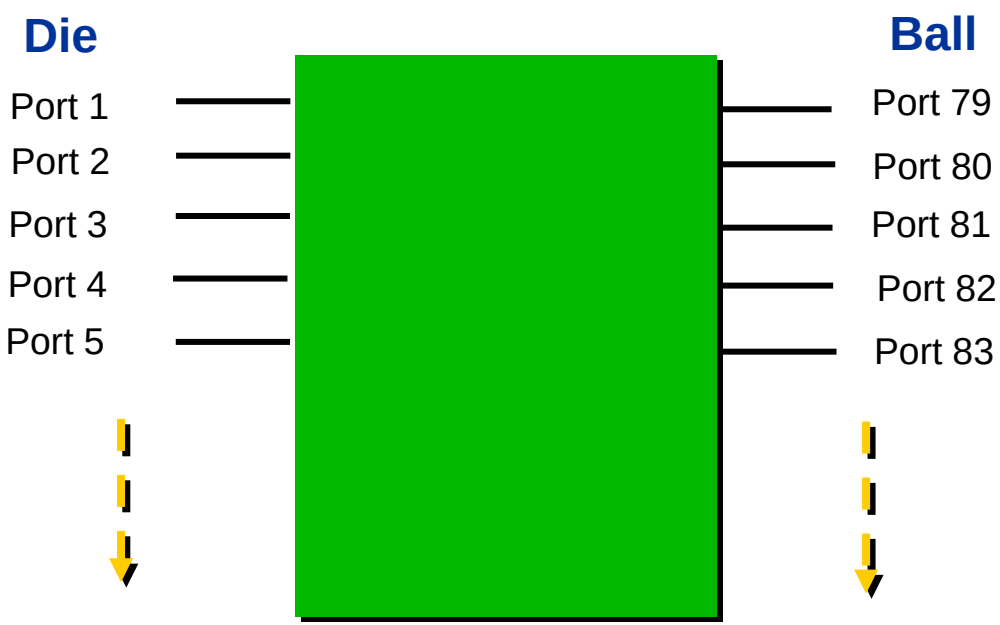
Task	Number of I/O Pins				Current Strength				I/O Location			
	1	10	40	Max	Min	Typ	Max		VIO	HIO	SSTL2	LVTTL3.3V
SSN Measurement	●	●	●	●	●	●	●	●	●	●	P1	P1
SSO Timing Push Out	●		●	●	●		●	●	●		P1	P1
SSO vol/voh Violation	●		●	●	●		●	●	●		P1	P1
Vref	●		●	●	●		●	●	●	●	P1	
Programmable Power/GND Ppins			●			●		●	●	●	P1	P1
			●			●		●	●			●
Indivudual vs. Adjacent Banks			●			●		●	●	●		●
Distribution of I/O Pins			●			●		●	●	●	●	●
SSN Measurement												

HSpice Models

- Encrypted HSpice Models For All I/O Pins
- Models Are Accompanied by Correlation Report & User Guide
- Package Models:
  - Distributed Models
  - Lumped Models

SSO Kit

- S-Parameter Models Using Sigrity Power SI
- HSpice Models Derived From S-Parameter Models Using Broadband Spice



HSpice Sub-Circuit Call

```
.subckt ss 1 2 3 4 5 6 7 8 9 10 11 12 13
                14 15 16
+17 18 19 20 21 22 23 24 25 26 27 28
                29 30 31
+32 33 34 35 36 37 38 39 40 41 42 43
                44 45 46 47
+48 49 50 51 52 53 54 55 56 57 58 59
                60 61 62 63
+64 65 66 67 68 69 70 71 72 73 74 75
                76 77 78 79
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+149 150 151 152 153 154 155 156 ref
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Other Modeling Collateral

- HSpice Kit
  - Library Of Transmission Line Models, Via Models & Connector Models, Correlated with Lab Measurements

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Design Services Partner Program

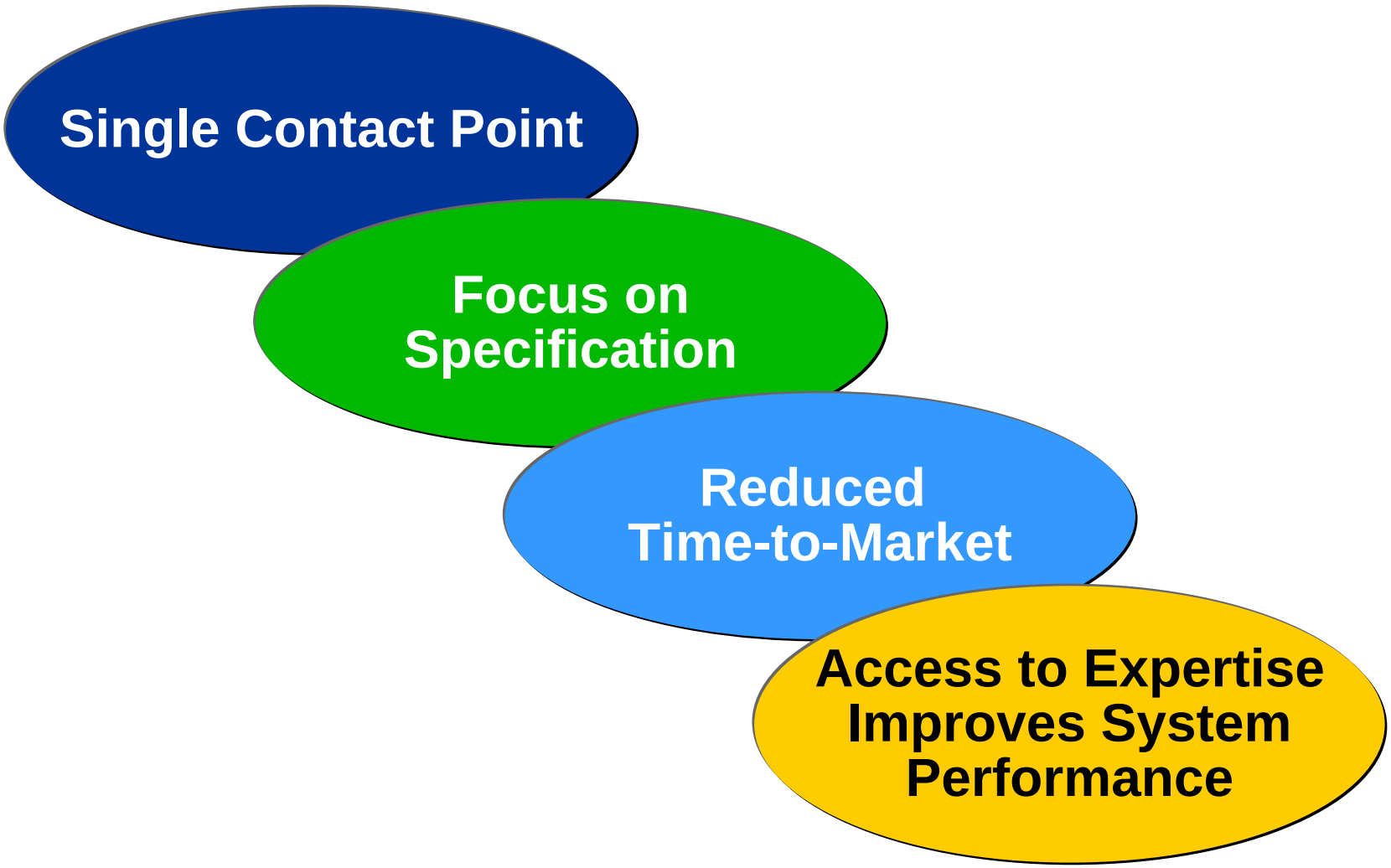
ACAP®
Altera Consultants Alliance Program

ALTERA®

Premise Behind Partner Program

- Altera Partners with Best-in-Class Engineering Firms to Provide Altera–Based Design Services for Mutual Customers
- Altera's Motivation
  - Expand Technical Resource Base
- Partner's Motivation
  - Worldwide Co-Marketing
  - Access to a Large Sales Channel
  - Access to Worldwide Customers

Benefits to Customers



Characteristics of Partners

- Altera Partners with Only the Best & Partners Are Limited in Number
- Characteristics of Partners:
  - Aligned Along Vertical Market Segments
  - Expertise at Architectural Level (Not at Socket Level)
  - Identified as Being Leaders in Their Segment
  - Significant Size & Financially Secure for Credibility
  - Already Known & Trusted by Customers
  - Worldwide Position
  - No Universal Pricing Method, Pricing Negotiated between Customer & Consultant
  - Supports Customer Directly

For More Information, Log onto www.altera.com, or Speak to Your Local Altera Sales Representative

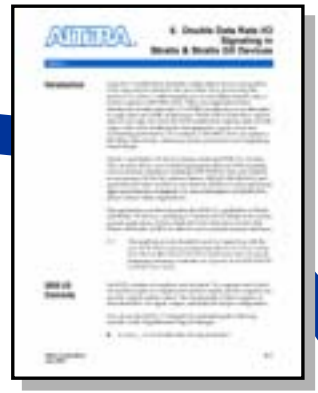
Additional Altera Resources

ALTERA®

Memory Interface Standard Deliverables

Handbook

- Device Description
- Electrical Parameters
- Device Timing



Application Note

- Interface Description
- Timing Analysis
- Electrical Analysis

Demonstration Board

- Demonstration Project
- Board Layout Guidelines
- Schematics/Gerbers
- Signal Integrity Analysis
- Documentation

MegaCore®

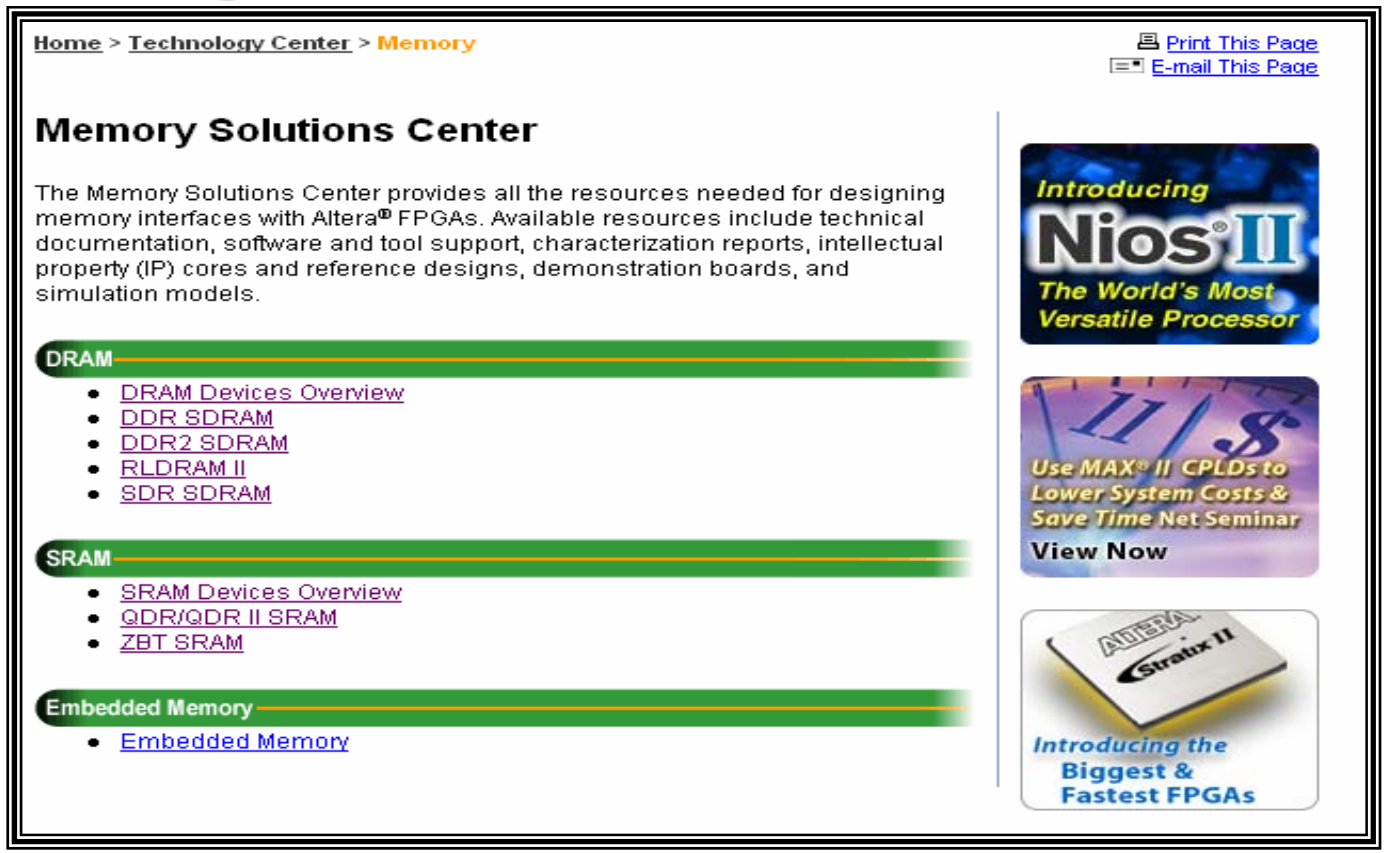
- User Interface
- Open Source Datapath
- System Timing Analysis
- Reference Design
- Constraints
- User Guide

QUARTUS® II

- Compilation Support
- Timing Models

ALTERA®

Memory Solutions Center



Web Site to Provide Easy Access to Memory Support Information

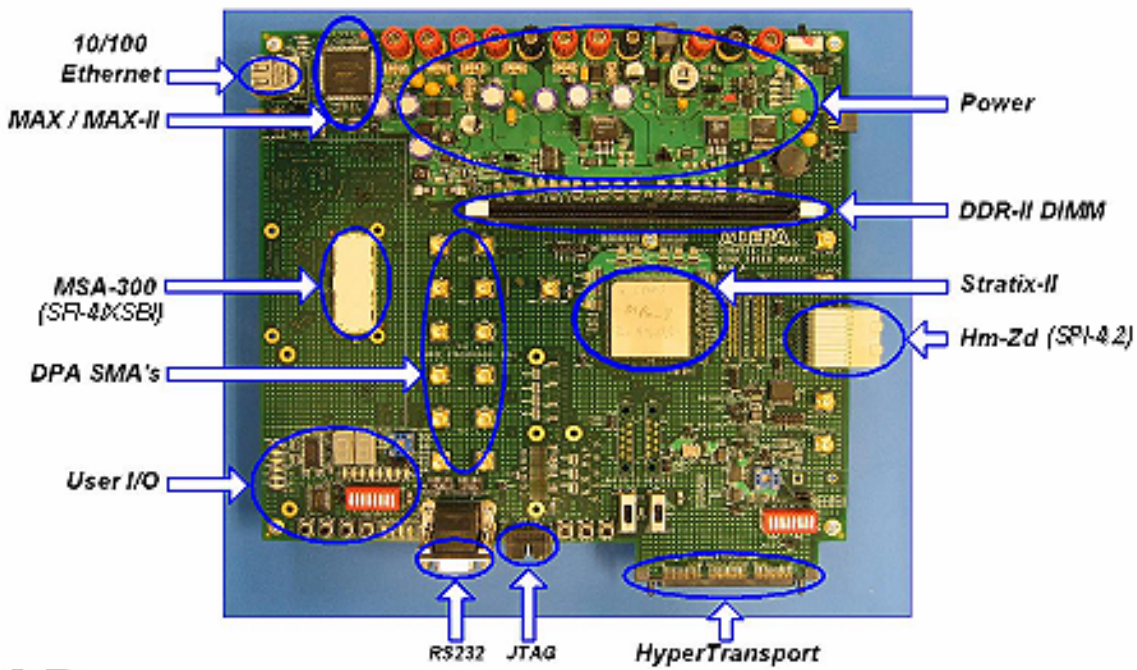
Benefits of Altera's Memory Solution

- Simplifies Memory Interface Design Process
  - Dedicated Circuitry in Silicon, Software & Tool Support
- Ensures First-Time Design Success
  - Hardware Reference Platform for Design Verification
- Reduces Design Cycles
  - IP Core Support, Detailed Documentation

Complete System-Level Solution

Stratix II High-Speed Development Board

- Designed for the Development of Applications that Incorporate High-Performance Interfaces
  - Stratix II EP2S60F1020C3 FPGA
  - External Connectors for a Broad Array of Applications



More Information

- Simultaneous Switching I/O Noise Guidelines for Stratix & Stratix GX FPGAs
- Minimizing Ground Bounce & Vcc Sag
  http://www.altera.com/literature/wp/wp_grndbnce.pdf
- Basics of Signal Integrity White Paper
  http://www.altera.com/literature/wp/wp_sgnlntgry.pdf
- High-Speed Board Layout Guidelines
  http://www.altera.com/literature/an/an224.pdf
- Guidelines for Designing High-Speed FPGA PCBs
  http://www.altera.com/literature/an/an315.pdf

More Information (cont.)

- Visit Altera's Memory Solution Center at: www.altera.com/memory

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Thank You !

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