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# **SOPC Design Using ARM-Based Excalibur Devices**

## **Outline**

- **ARM-based Devices Overview**
- **Embedded Stripe**
- **Excalibur MegaWizard**
- **Verification Tools**
  - **Bus Functional Model**
  - **Full Stripe Model**
- **Configurations**
- **Software Tools**
- **Applications Examples**
- **Summary**

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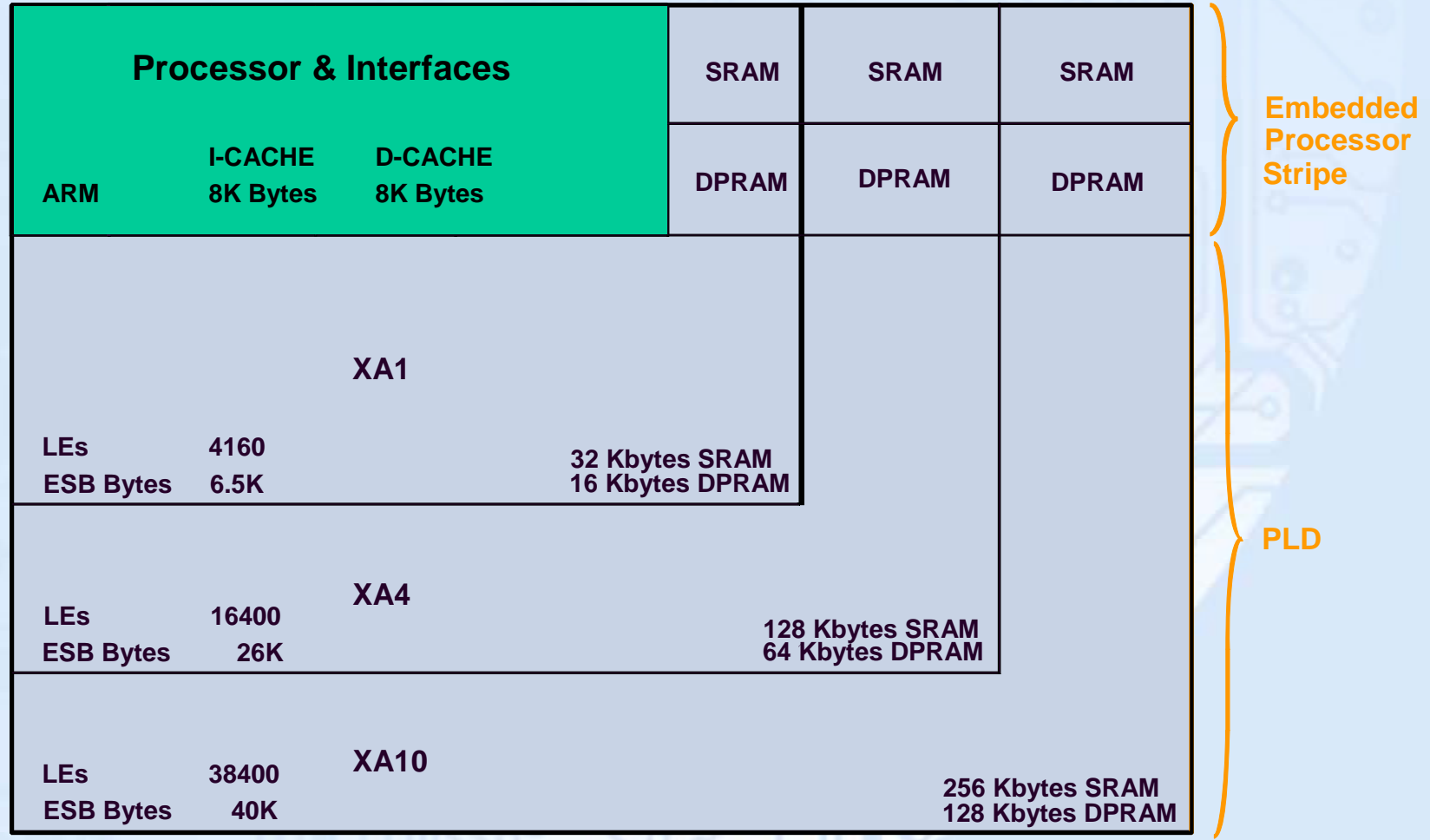
# **ARM-Based Devices Overview**

# Features

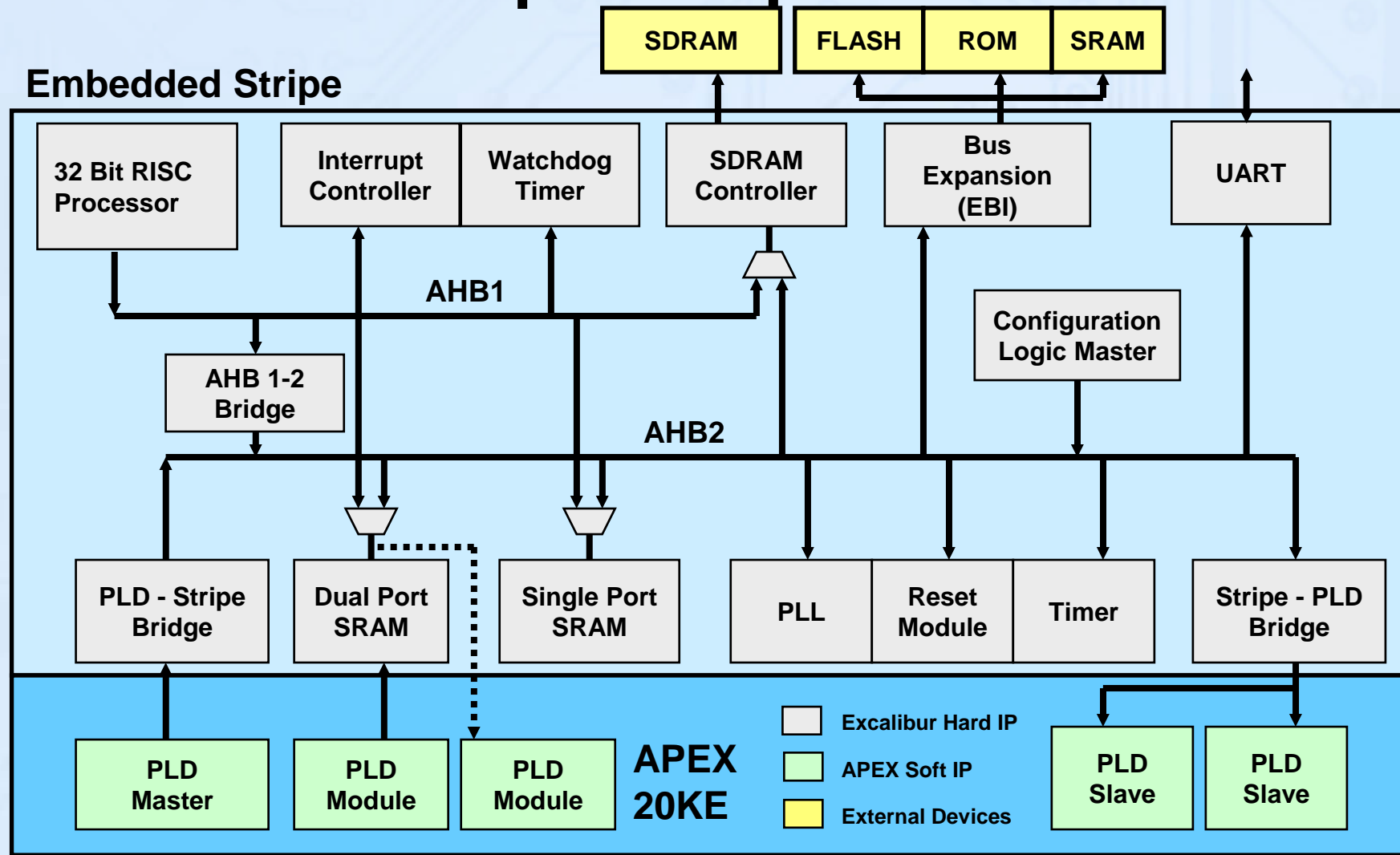
- **32 Bit RISC Processor**
  - 200 MHz ARM922T™
- **High Performance .18 μm 8LM TSMC Process**
- **AMBA™ Bus Architecture**
  - Industry Standard Bus Architecture
- **Stripe Memory**
  - Single Port and Dual Port
- **External Memory**
  - SDRAM, DDRSRAM, FLASH, SRAM



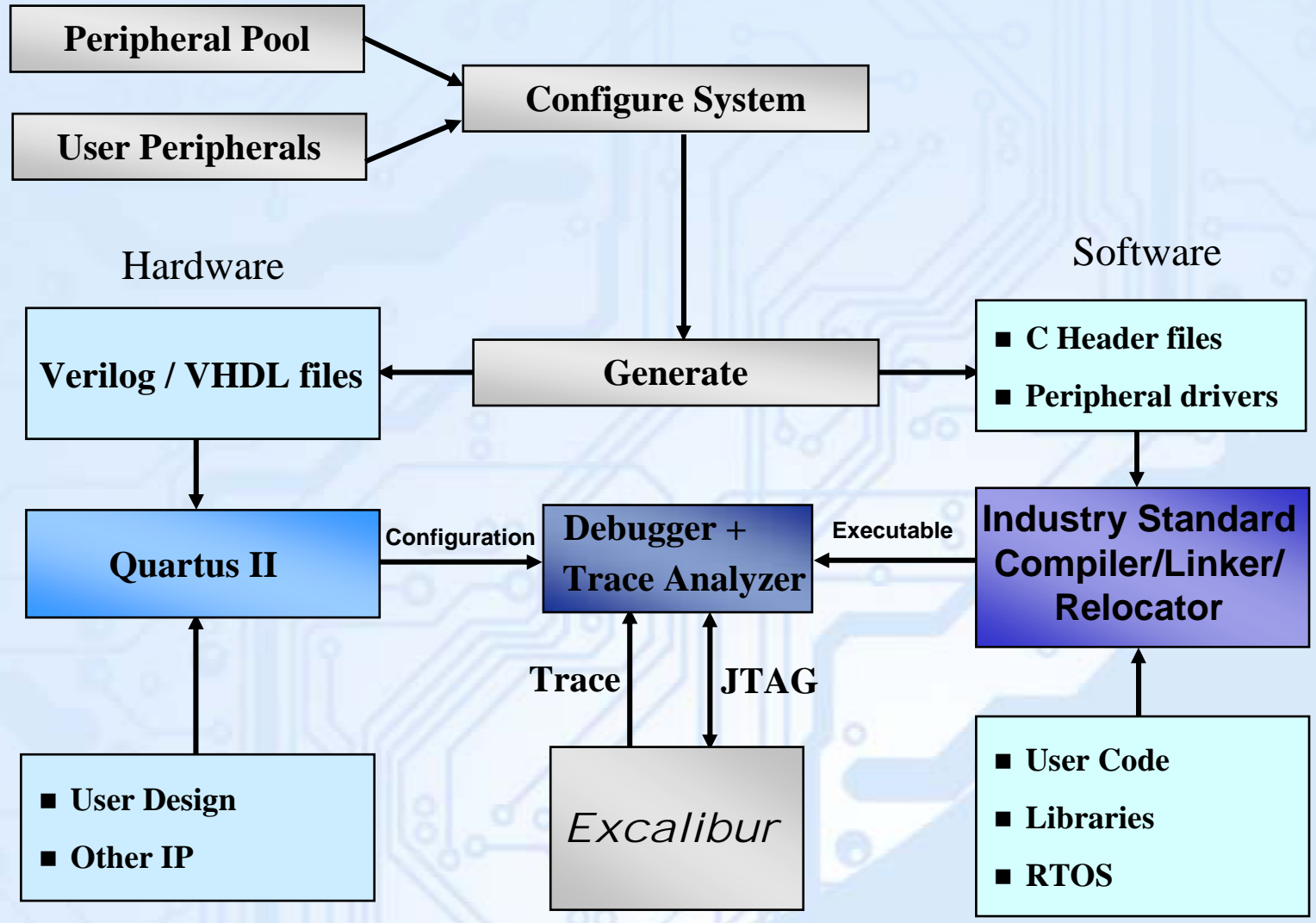
# Hard Processor PLD Architecture



# Excalibur Stripe Components



# Excalibur Work Flow





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# **Embedded Stripe**

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## **ARM922T Processor**

- **Based on the ARM922™ (ARM920™ Derivative) and Incorporating the ARM9TDMI™**
- **High Speed Cache (8KB Instruction + 8KB Data)**
- **Single Cycle Repeat-rate SRAM and DPRAM**
- **MMU Facilitates the Implementation of Real-time Operating Systems (RTOS)**
- **200MHz on Altera® 1P/8M, 0.18u Process at TSMC**
- **Advanced Built-in System Debug Features**

## ARM92TDMI

- Based on ARM9TDMI core
  - Five stage pipeline
  - Harvard bus architecture
  - CPI of 1.5

### ARM9 -

- T** - Thumb Architecture Extension
- D** - Core has Debug Extensions
- M** - Core has an enhanced Multiplier
- I** - Core has EmbeddedICE Logic Extension

# **AMBA High Performance Bus (AHB)**

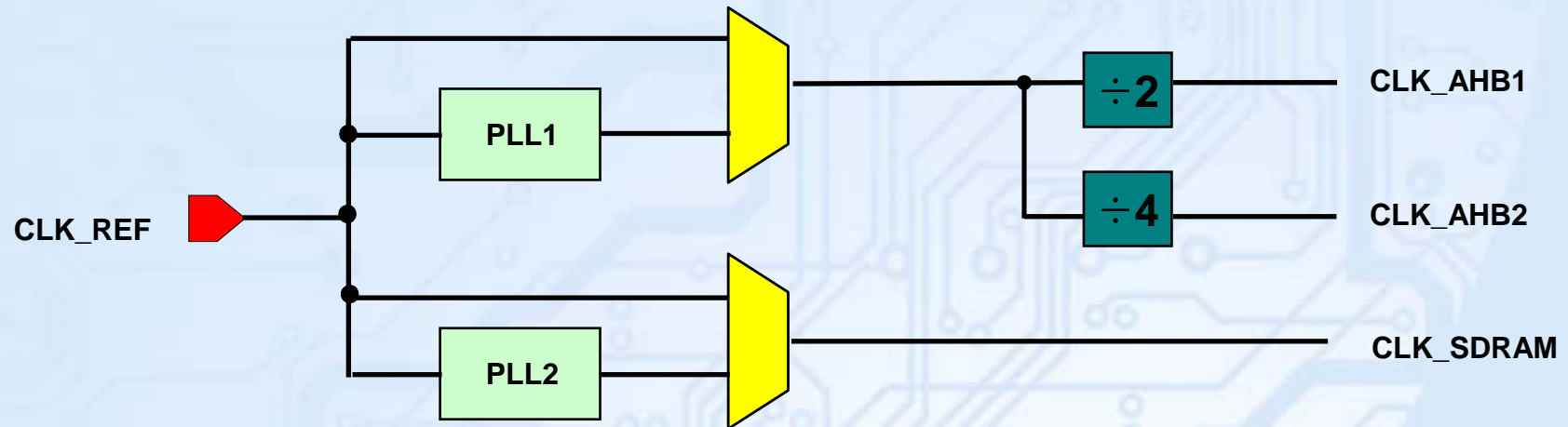
- **AMBA - Advanced Micro-controller Bus Architecture**
- **Connects Embedded Stripe and PLD Devices**
- **200MHz Maximum Clock Rate**
- **32 Bit Wide Pipelined Bus**
  - **Burst transfers - one cycle per data word**
  - **Non-tristate implementation**
- **Multi-master With Distributed Address Decoding**
  - **Single-cycle bus master handover**
- **Split Transactions Extensions**
  - **Needed to fully exploit bus bandwidth in a multi-master bus**

# Stripe PLL's

- **Stripe PLL's Provide Clock Boost Multiplication Only**
  - Default power-up operation is bypass
  - Program control registers through configuration logic or the embedded processor
  - State machine control to put PLL in bypass mode if lock is lost
  - Can change PLL frequency with proper software control
- **PLL1**
  - Clock for processor and peripheral bus
  - Up to 400 Mhz operation divided by 2 or 4
- **PLL2**
  - Clock for the SDRAM controller
  - Up to 266 Mhz operation

# Stripe PLL's

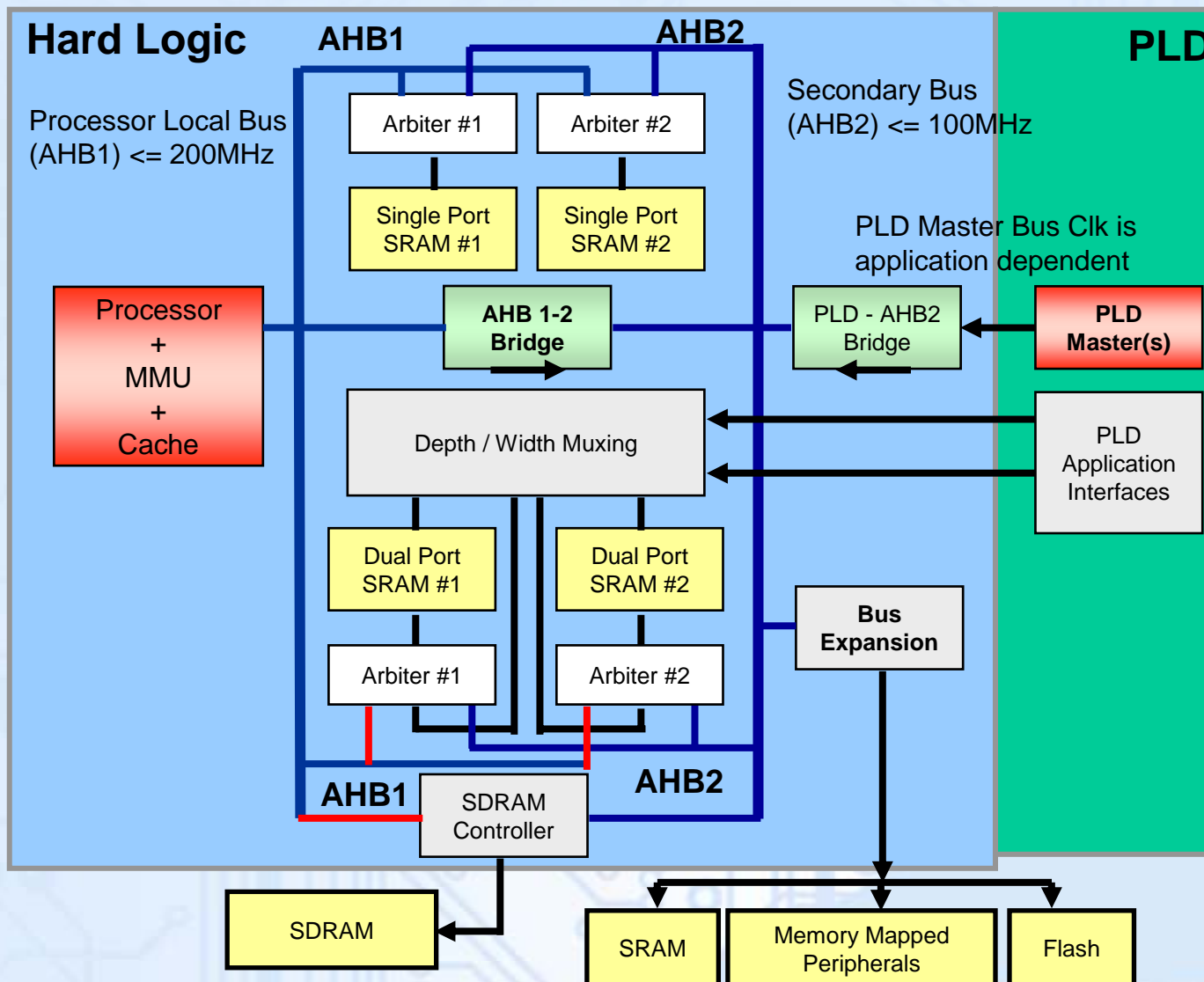
- Stripe Contains 2 PLL's



- PLL 1 & PLL 2 are similar to APEX PLLs

- $F_{out} = CLK\_REF \text{ (MHz)} * M / (N * K)$  where M, N, K are integers
- PLLs can be bypassed

# Excalibur Memory Hierarchy



# Single Port SRAM

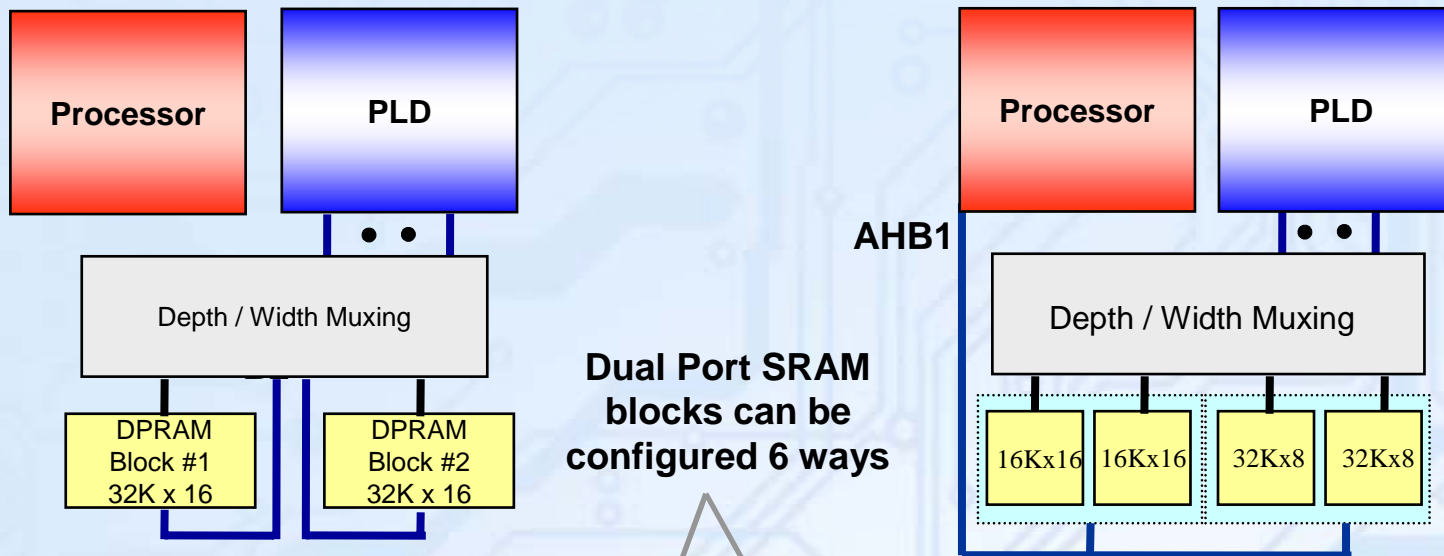
- **Stripe Memory**
  - 2 blocks of independent addressable memory available on AHB1 or AHB2 bus
  - 32, 128, or 256 Kbytes total depending on device size
- **Arbiter Resolves Competition Between AHB1 and AHB2 Interfaces for Access to the SRAM**
  - Defaults to fixed round-robin scheme with fairness
  - Supports locked transfers
- **Each SRAM Block Is Byte Addressable**
- **Supports Big or Little Endian Transfers**



## **Dual Port SRAM**

- **Stripe Memory**
  - 2 blocks available on AHB1 or AHB2 bus
  - 16, 64, or 128 Kbytes depending on device size
  - Each block can itself be configured as 2 blocks for a total of 4 independent addressable DPRAM
- **Available From AHB1, AHB2, or PLD**
  - Arbiter controls access
- **Each Block Is Byte Addressable**
- **Supports Various Widths and Depths**

# Dual Port SRAM Configurations



Dual Port SRAM blocks can be configured 6 ways

	Dual Port SRAM Block Configurations (Excalibur1000)
AHB Interface	-
PLD Interface	1 x 16k x 32 1 x 32k x 16 2 x 16k x 16 1 x 64k x 8 2 x 32k x 8 32k x 16 Dual Port (*)

(\*) - Configuration shown here

	Dual Port SRAM Block Configurations (Excalibur1000)
AHB Interface	128 Kbytes (16Kx16) 256 Kbytes (32Kx8)
PLD Interface	1 x 16k x 32 1 x 32k x 16 2 x 16k x 16 (*) 1 x 64k x 8 2 x 32k x 8 (*) 32k x 16 Dual Port

(\*) - Configurations shown here

# SDRAM Controller

- **Stripe Contains a Controller for SDRAM or DDR SDRAM External Memory**
  - Either 16 or 32 bit SDRAM or DDR SDRAM can be connected but not both
- **Runs Asynchronously to AHB1 or AHB2**
- **Supports Byte, Half-word, and Word Transfers**
- **Addressing**
  - AHB buses are byte addressed, DRAM is bit addressed
  - DRAMS have row, column, and bank address
  - Number of row and column bits depends on memory used
- **Supports 2 Blocks and up to 512 Mbytes Total of External DRAM**
- **Supports PC100/133 SDR SDRAMs and PC200/266 DDR SDRAMs**
- **SDRAM must be initialized through software control**

## **Expansion Bus Interface (EBI)**

- **Provides Capability to Interface to External Memory Mapped Devices**
- **Different Sizes and Types Available**
- **Rate-Adaptation Between Flash Memories or Memory Mapped Peripherals and AHB2 Bus Masters**
- **Four Chip Select Outputs**
  - **Each Address Space Can Be Configured to Operate in an 8- or 16-Bit Mode.**
  - **Bus Timing and Interface Signals Can be Configured by a Bus Master**
- **Supports Split Bus Transactions**
  - **Prevents Stalling of Other AHB2 Bus Masters**
- **Support both synchronous & asynchronous mode**

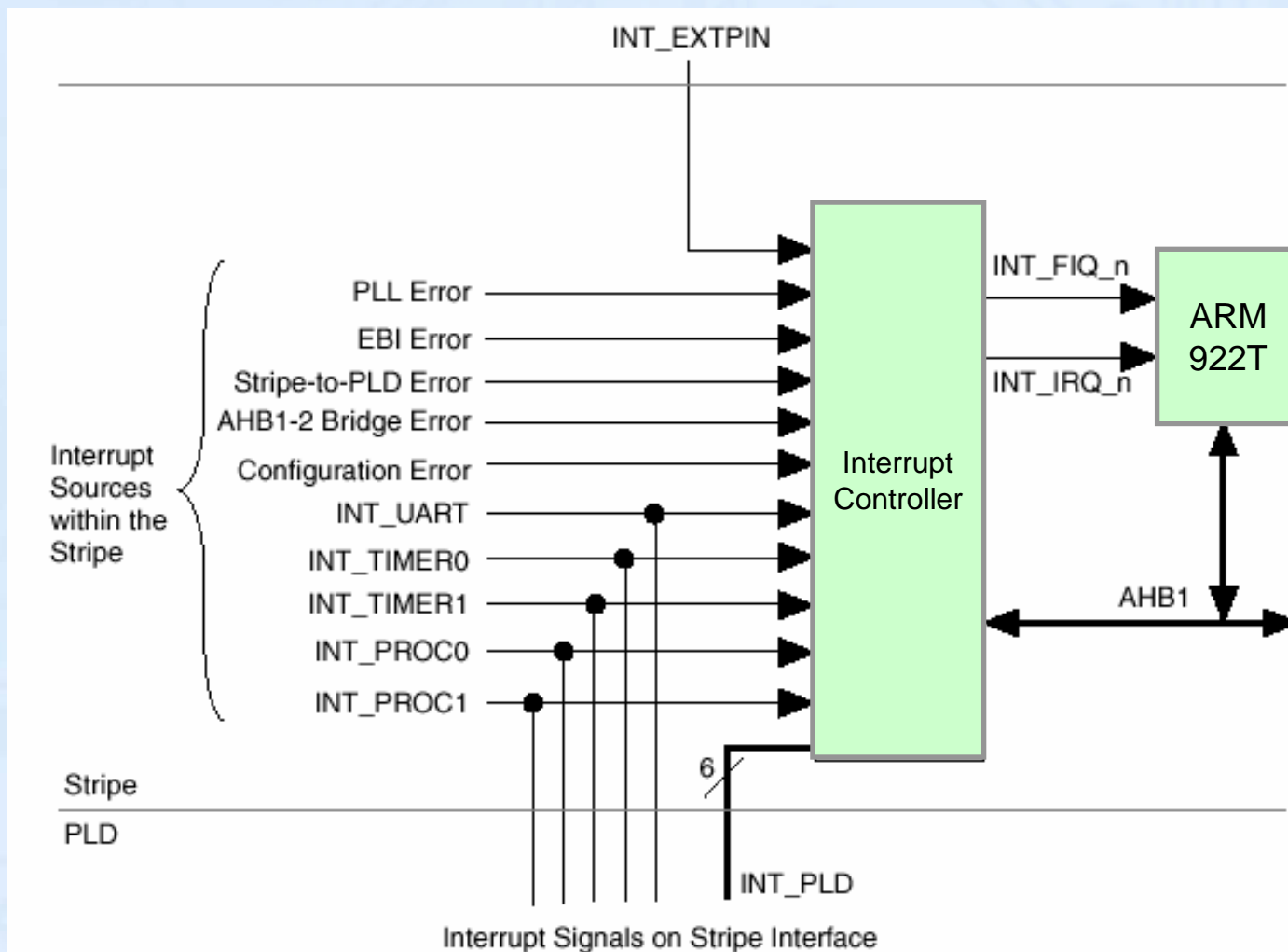
# UART

- 5 to 8 data bits
- 1 or 2 stop bits
- Even, odd, stick, or no parity
- 75 to 230,400 baud rate
- 16-byte transmit FIFO
- 16-byte receive FIFO.
- Programmable baud generator
- Internal diagnostic capabilities
- Modem communication support

# **Interrupt Controller**

- **User Configurable to Three System Modes**
  - **Interrupt Sources Can Arise From Stripe and PLD**
- **Priority and Enabling Scheme**
  - **All Interrupts Disabled on Power-up**
  - **Sets Priority on Interrupt Sources**
  - **Enables or Disables Individual Interrupt Sources**

# Block Diagram



## **Watchdog Timer**

- **Protects the System against Software / Hardware Failures**
- **One-shot Timer Resets Entire Chip When It Expires**
- **32-bit Register Interface Provides User-selected Timeouts**
  - **Up to 30s With a 33MHz Clock**



# Timer

- **Dual-Channel Timer**
- **32 Bit Prescaler**
- **32 Bit Timer Register**
- **Three Operating Modes**
  - **Free running interrupt (heartbeat)**
  - **Software controlled start/stop (interval timer) with interrupt on limit**
  - **One-shot interrupt after programmable delay**

## **Reset & Mode Control**

- **PLD power-on reset**
- **Resets from external sources**
  - **Configuration pin nCONFIG**
  - **External reset pin (bi-directional open drain pin, supplying reset output to flash devices)**
  - **External power-on reset**
- **Resets from internal sources**
  - **Software watchdog timer reset**
  - **JTAG module**
  - **Configuration error**

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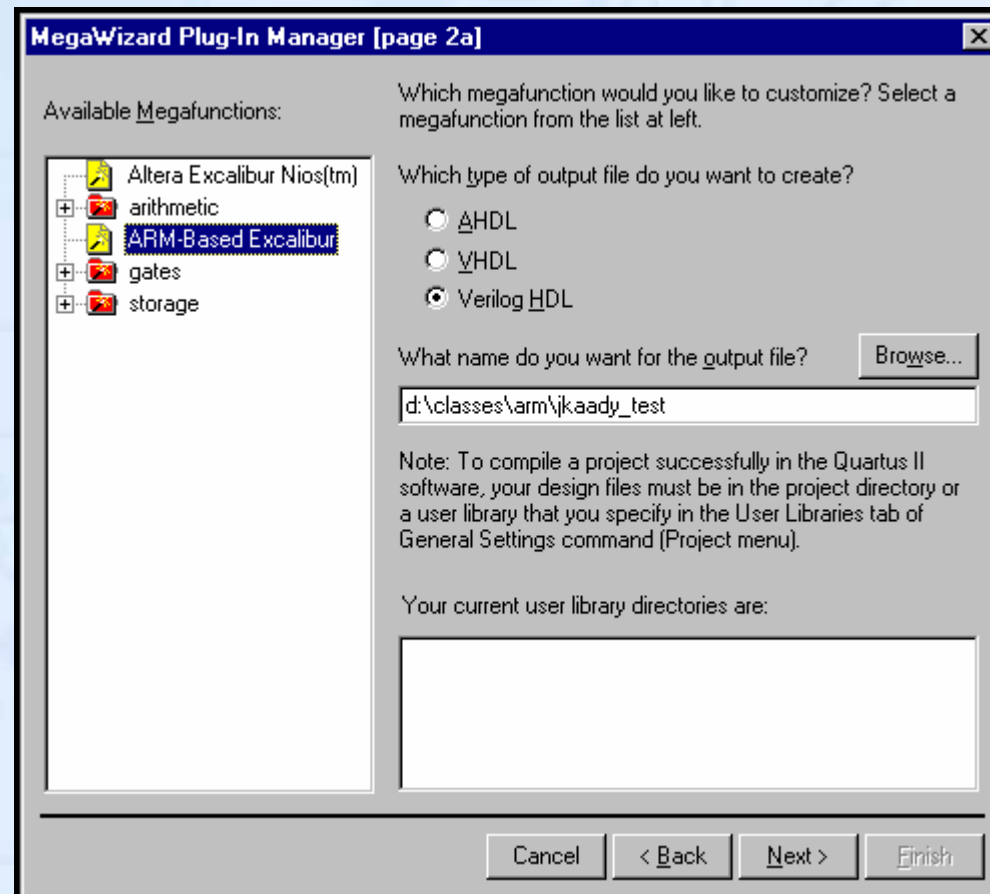
# **Excalibur ARM MegaWizard**

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# Excalibur MegaWizard

- Select ARM<sup>®</sup>-Based<sup>™</sup> Excalibur<sup>™</sup>
  - Easily create the desired stripe configuration



# MegaWizard

Select family and device

Hold processor in reset?

Boot from FLASH?

Endianess

Reserve pins

Megawizard Plug-In Manager - Excalibur [Page 3 of 7]

This page allows you to select and configure the Excalibur device to suite your particular application. It also allows you to enable or disable those 'stripe' modules that require external access and therefore pins to be reserved on the Excalibur device.

Select Excalibur family: Excalibur\_ARM  
Select available device: EPXA10

Reset operation

**If the processor is held in reset, it can only be released by a write to the 'stripe' Boot control register by one of its two remaining bus masters.**

Do you want the processor to be held in reset?  
 Do you want to Boot from FLASH?

Byte order

Little endian  Big endian

Reserve pins

Do you want to reserve pins for any of the following 'stripe' modules?

<input checked="" type="checkbox"/> EBI (FLASH)	Outputs: Slow slew rate	Inputs: 3.3V LVTTTL
<input checked="" type="checkbox"/> SDRAM	Outputs: Fast slew rate	Inputs: SSTL 2
<input checked="" type="checkbox"/> UART	Outputs: Slow slew rate	Inputs: 3.3V LVTTTL
<input type="checkbox"/> Trace	Outputs: Fast slew rate	No Inputs

Cancel < Prev Next > Finish

# MegaWizard

Select the AHB2 to  
PLD bridges

Select the Interrupts

Megawizard Plug-In Manager - Excalibur [Page 4 of 7]

This page allows you to configure the interface between the 'stripe' and the PLD.

Bridges

**Note: The PLD-TO-STRIPE bridge allows a master or masters in the PLD to access resources in the 'stripe'. Similarly the STRIPE-TO-PLD bridge allows masters in the 'stripe' access to resources in the PLD.**

Do you want to use the STRIPE-TO-PLD bridge (Master Port)?

Do you want to use the PLD-TO-STRIPE bridge (Slave Port)?

Interrupts

**Note: If you choose to implement an interrupt controller within the PLD then you must also select the mode of operation for the main interrupt controller (in the 'stripe'), which will determine how these PLD interrupt request signals are treated.**

**If you select Mode 3 you will also need to configure the PLD\_MS register in the 'stripe'. Please see the Excalibur data sheet for more details.**

Do you want to use the STRIPE-TO-PLD interrupt sources?

Do you want to use the PLD-TO-STRIPE interrupt sources?

Select PLD interrupt mode: Mode 3 - Six individual requests

Trace / Debug

Do you want to use processor debug extensions?

Do you want to use processor trace extensions?

Cancel < Prev Next > Finish

# MegaWizard

External clock reference

AHB1 / AHB2 clock settings

SDRAM clock setting

Megawizard Plug-In Manager - Excalibur [Page 5 of 7]

This page allows you to configure the clocks (PLL's) for the processor and SDRAM (if required).

External clock reference

Enter external reference frequency  MHz

AHB1 / AHB2 clock settings

Bypass PLL1

Enter desired AHB1 frequency  MHz

AHB1 frequency achieved: **198.0000 MHz**

AHB1 VCO frequency: 396.0000 MHz (300MHz optimal)

Select AHB2 frequency:  MHz

SDRAM clock settings

Bypass PLL2

**Note: The desired frequency for SDRAM refers to the frequency of the SDRAM\_CLK pin. For DDR SDRAM the operating frequency is double this.**

Enter desired SDRAM frequency  MHz

SDRAM frequency achieved: **132.0000 MHz**

SDRAM VCO frequency: 264.0000 MHz (300MHz optimal)

Serial Programming

Are you using a serial EEPROM configuration device?

Choose your device:

Enter your programming frequency  MHz

Cancel < Prev Next > Finish

# MegaWizard

Enter the base address & size

Automatic checking for overlapping regions or incorrect base address

Megawizard Plug-In Manager - Escalibur [Page 6 of 7]

This page allows you to configure all of the memory regions of the Escalibur device. You can adjust the base address and size of any region, together with the region parameters (if any), by editing or selecting the controls within the 'Memory map' area.

Memory map	Address	Size	Other
Registers	7FFFC000	16K	
SRAM0	00000000	16K	
SRAM1	00040000	16K	>
DPRAM0	00060000	64K	
DPRAM1		OFF	
SDRAM0	00800000	8M	
SDRAM1		OFF	
EB0 (FLASH)	00000000	32K	
EB1		OFF	
EB2		OFF	
EB3		OFF	
PLD0		OFF	
PLD1		OFF	
PLD2		OFF	
PLD3		OFF	

No Additional Settings for SRAM1

Enter an address which is a multiple of 16Kbytes (4000 Hex)  
Address fields shown in red are currently overlapped. Please correct before continuing.  
The size of the memory region must be an exact multiple of its base address.

Cancel < Prev Next > Done



# MegaWizard

SRAM0,SRAM1  
DPRAM0, DPRAM1  
Memory Map

Combine dual port?

DPRAM0 setting  
DPRAM1 setting

This page allows you to configure all of the memory regions of the Excilbur device. You can adjust the base address and size of any region, together with the region parameters (if any), by editing or selecting the controls within the 'Memory map' area.

Memory map	Base Address	Size
Registers	7FFFC000	16K
SRAM0	00020000	128K
SRAM1	00040000	128K
DPRAM0		OFF
DPRAM1	00080000	128K
SDRAM0	00800000	8M
SDRAM1		OFF
EB0 (FLASH)	00000000	32K
EB1		OFF
EB2		OFF
EB3		OFF
PLD0		OFF
PLD1		OFF
PLD2		OFF
PLD3		OFF

**Note:** The size of the dual-port SRAM block (given below) within the 'stripe' memory map will vary with the configuration.

Combine dual port RAMS

Combined settings

DPRAM0 configuration: 32K x 32

Outputs registered

DPRAM0 settings

PLD Access: 1 x dual port 32K x 16

Outputs registered

DPRAM1 settings

PLD Access: 1 x single port 32K x 16

Outputs registered

Sizes

DPRAM0 block size: OFF

DPRAM1 block size: 128KByte

No errors detected.

Cancel Prev Next Finish

# MegaWizard

Memory Type  
Timing Parameter  
Address bits

SDRAM0, SDRAM1  
Memory map

Select device and port  
width

Click on the Show  
details button

Megawizard Plug-In Manager - Excilbur [Page 6 of 7]

This page allows you to configure all of the memory regions of the Excilbur device. You can adjust the base address and size of any region, together with the region parameters (if any), by editing or selecting the controls within the 'Memory map' area.

Memory Region	Base Address	Size	Port Width
Registers	7FFFC000	16K	
SRAM0	00020000	16K	
SRAM1	00040000	16K	
DPRAM0			OFF
DPRAM1	00080000	128K	
SDRAM0	00800000	8M	>
SDRAM1			OFF
EBI0 (FLASH)	00000000	32K	
EBI1			OFF
EBI2			OFF
EBI3			OFF
PLD0			OFF
PLD1			OFF
PLD2			OFF
PLD3			OFF

No errors detected.

Cancel Prev Next Finish

Custom

SDRAM memory type  
 SDR  DDR

SDRAM timing

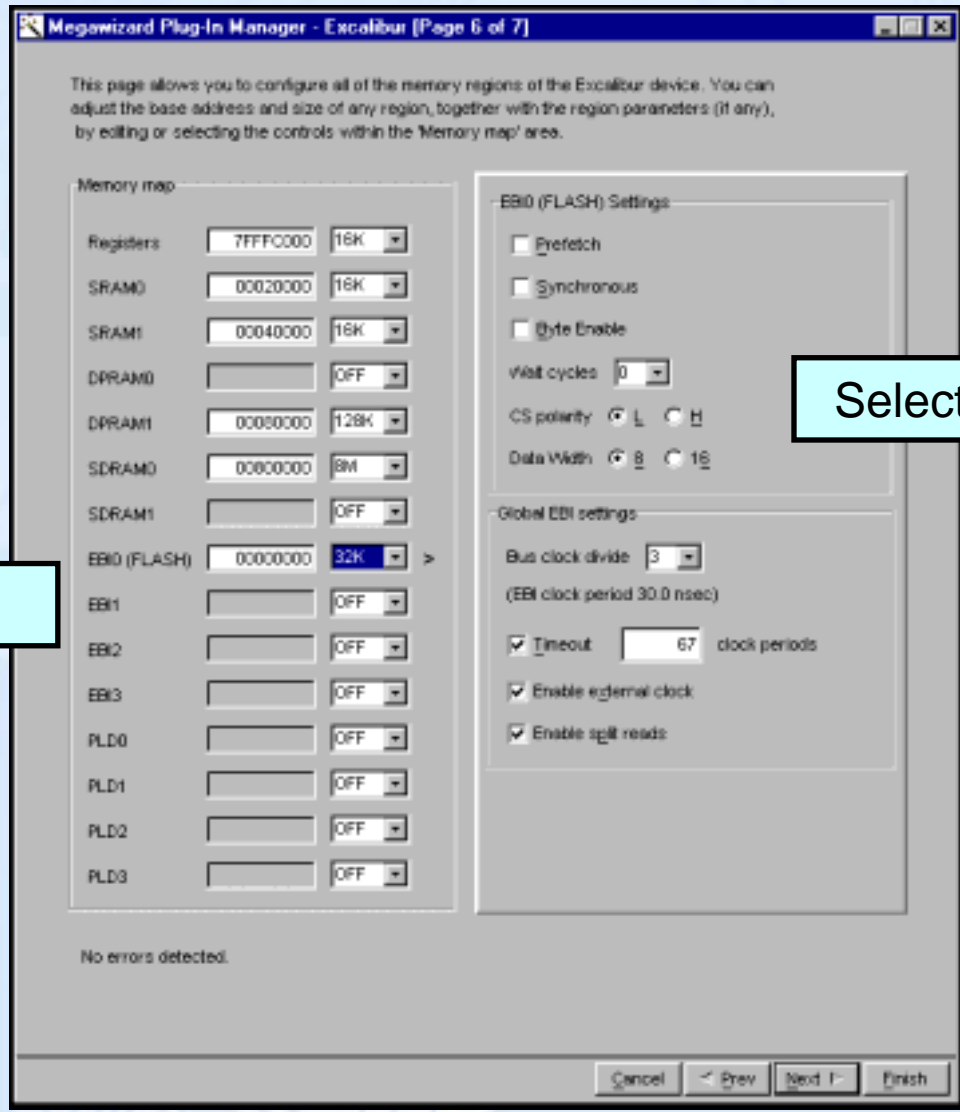
Active to Read or Write delay (RCD) 20 ns  
Active to Precharge command (RAS) 45 ns  
Active bank A to Active bank B command (RRD) 15 ns  
Precharge command period (RP) 20 ns  
Write recovery time (MR) 15 ns  
Active to Active command period (RC) 66 ns  
Auto Refresh period (RFC) 75 ns  
Auto Refresh Interval (RFSH) 15625 ns  
CAS latency (CL) 2  
Burst Length (BL) 4

SDRAM size

Number of row address bits (ROW) 12  
Number of column address bits (COL) 8  
Number of bank address bits (BA) 2

Cancel OK

# MegaWizard

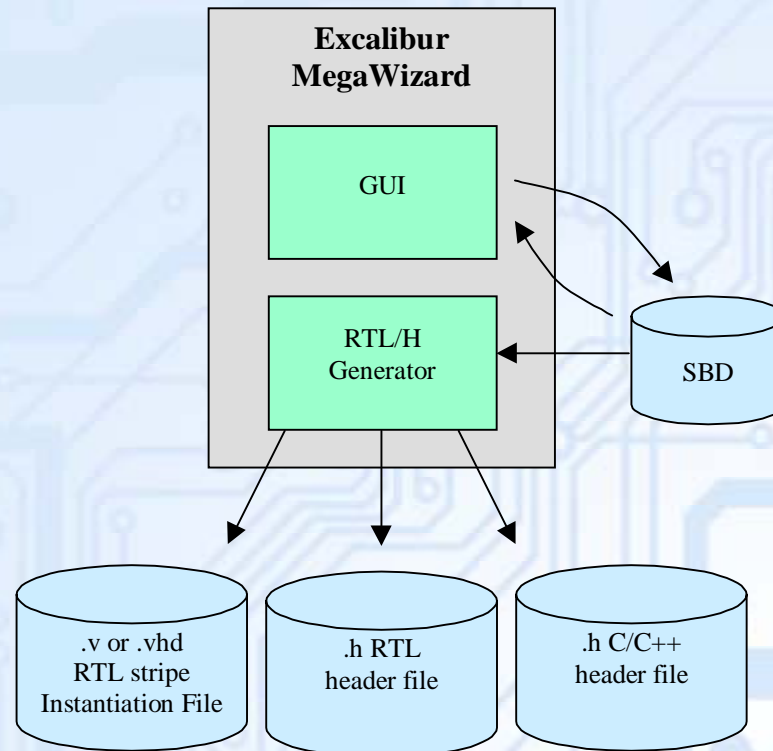


EB0-3 Memory map

Select device settings

# Excalibur Megawizard

- A Megawizard in Quartus II will assist the customer to define the Memory Map, etc



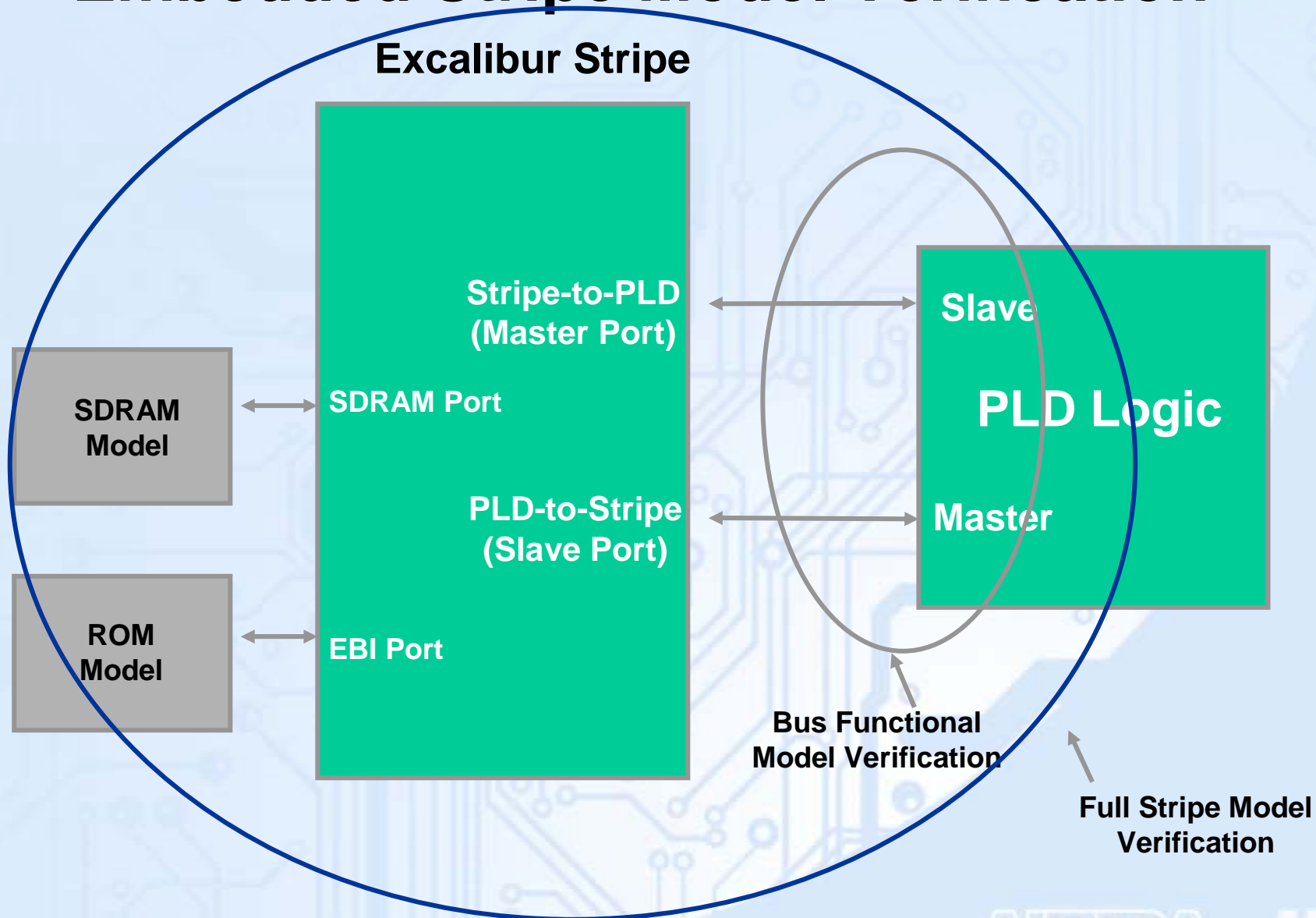
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# **Verification Tools**

## **Bus Functional Model**

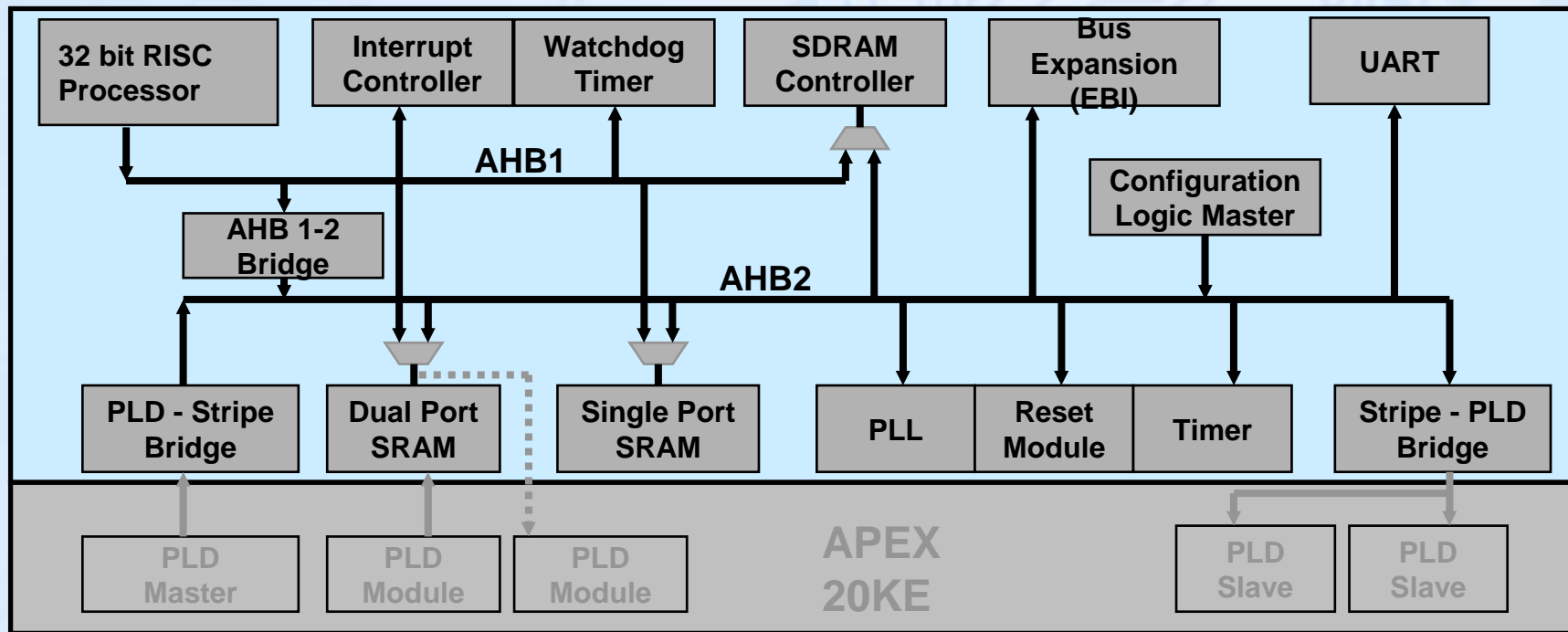
- **Verifies the ability of PLD Peripherals to AHB Protocol**
  - **AMBA AHB Masters and Slaves**
- **Models AHB Transactions**
  - **Includes Master Port and Slave Port Bus Transactors**
  - **Models AHB Master and AHB Slave - Accepts and Transmits AHB Protocol Signals**
  - **Does Not Model**
    - **Excalibur ARM Stripe**
    - **Stripe-PLD Bridge**
    - **PLD-Stripe Bridge**

# Embedded Stripe Model Verification



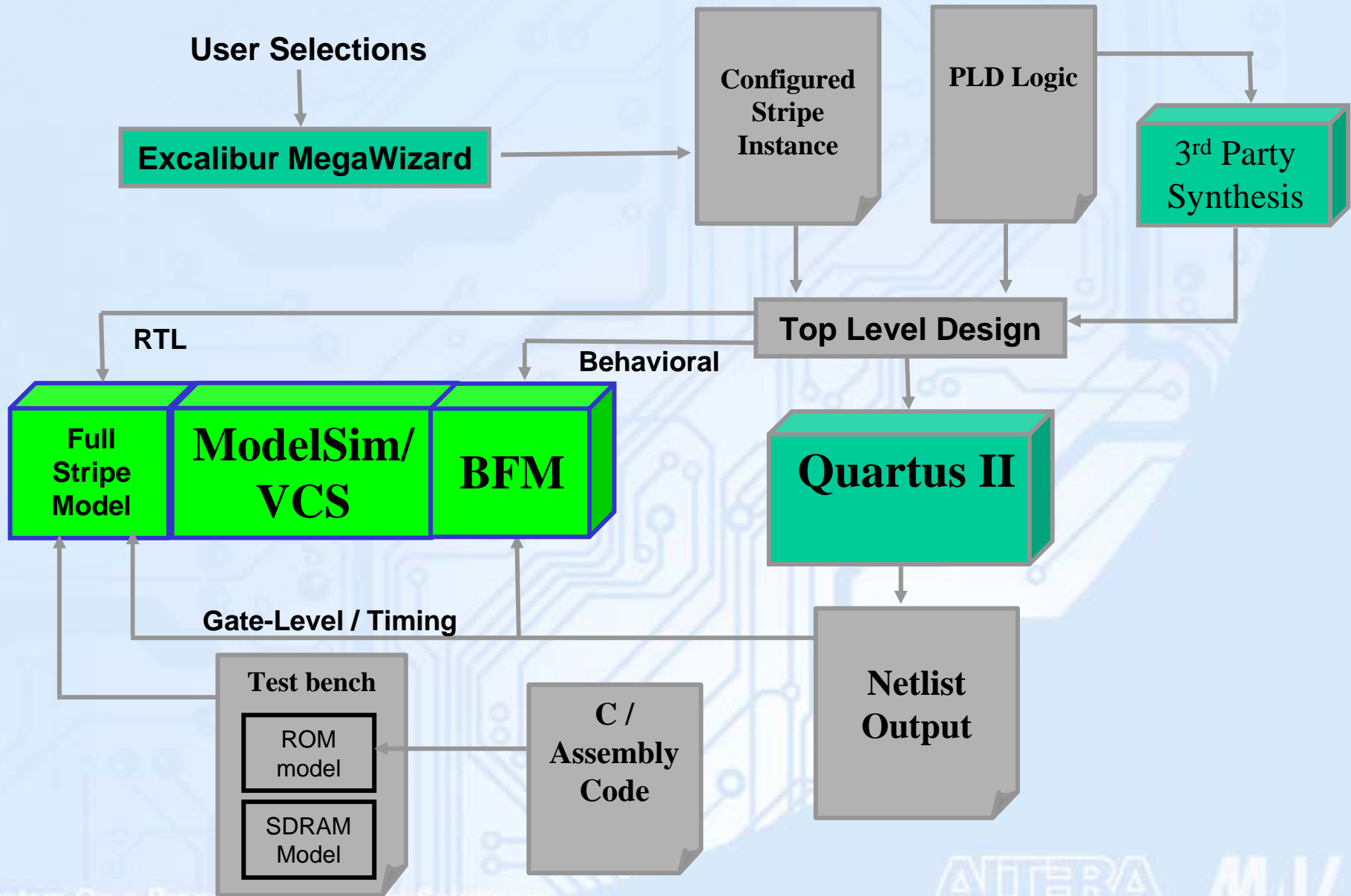
# Cycle Accurate Stripe Model

- Processor
- Timer
- Interrupt Controller
- UART
- EBI
- DPRAM, SRAM
- SDRAM Controller
- AHB1-2 Bridge
- Stripe-to-PLD Bridge
- PLD-to-Stripe Bridge
- PLLs (limited model of behavior)
- PLD Configuration Not Modeled





# Verification Tool Flow



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# **Configuration Methods**

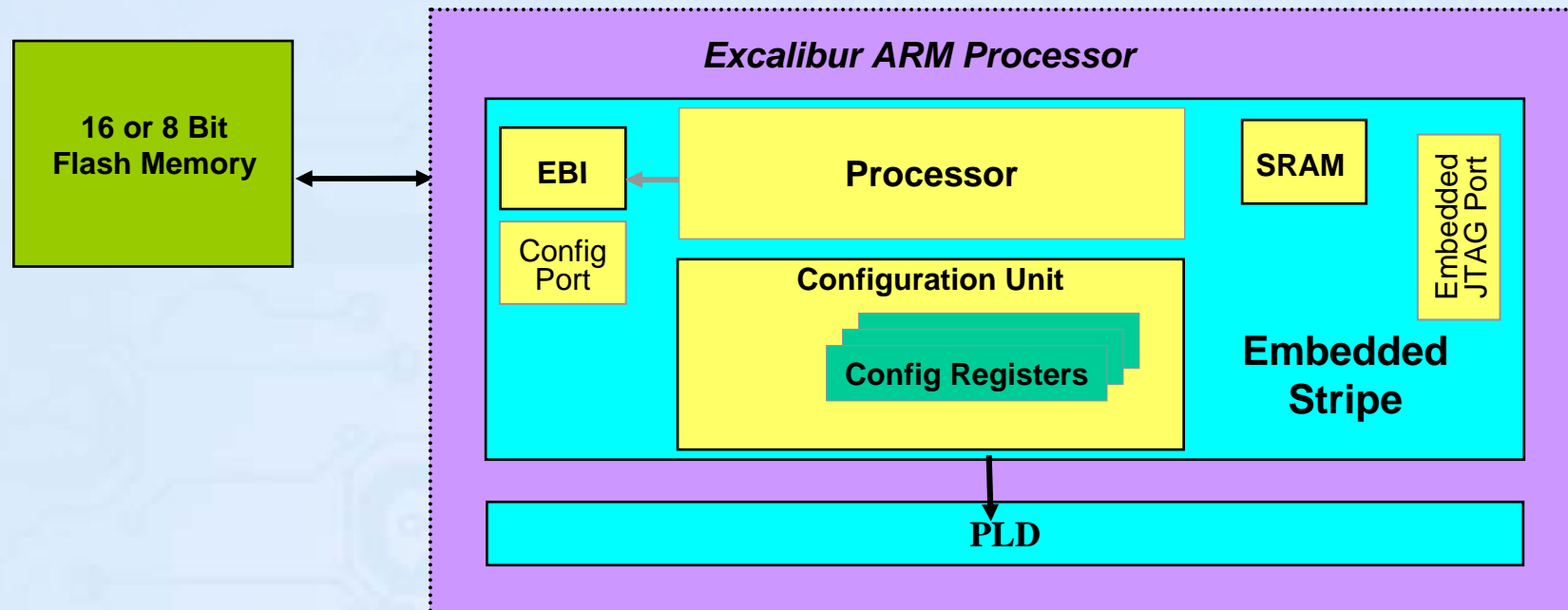
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# Configuration Methods

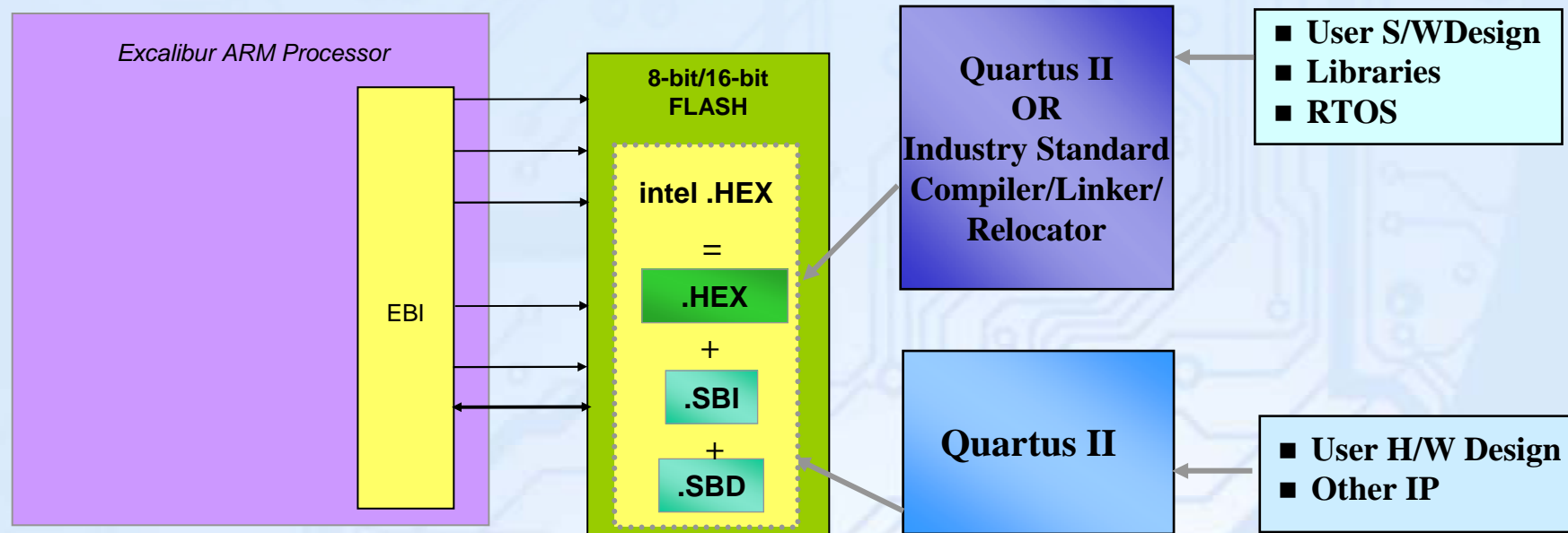
- **Processor Centric**
  - Boot From Flash
  - Possible for Multiple PLD Images
- **PLD Centric**
  - Passive Serial
  - Passive Parallel
  - JTAG

# Processor-Centric Configuration Mode



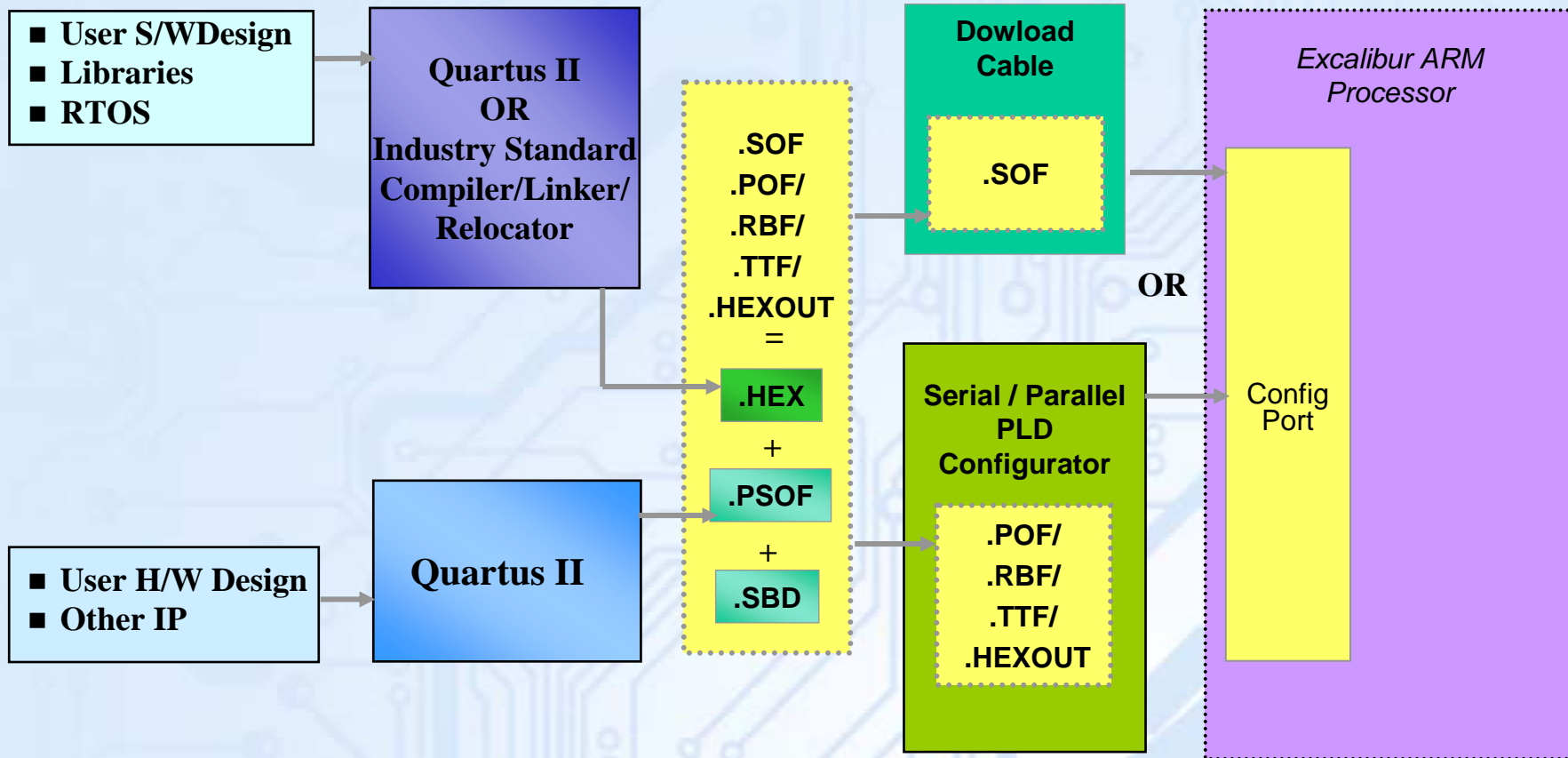
- Processor boots from External Flash and Configures Embedded Stripe and PLD
- First-time flash programming can be done using JTAG

# Configuration File in Flash



- The intel .HEX programming file is generated by a combined effort of Quartus II and external softwares
  - The .HEX component is made by Quartus II in Software Mode or by external software tool
  - The .SBI component is made by Quartus II in Hardware mode
  - The .SBD component is made by the Excalibur MegaWizard

# Configuration Files in PLD-centric Mode



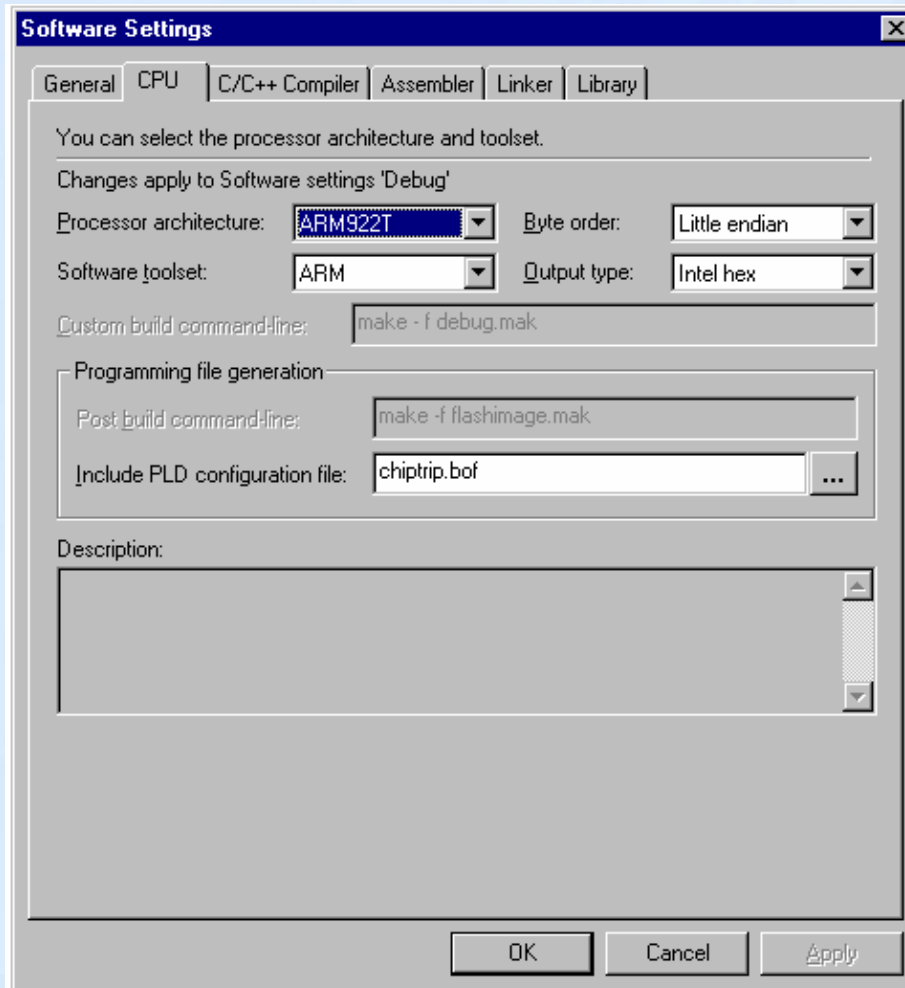
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# **Software Tools**

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# Quartus II SoftMode



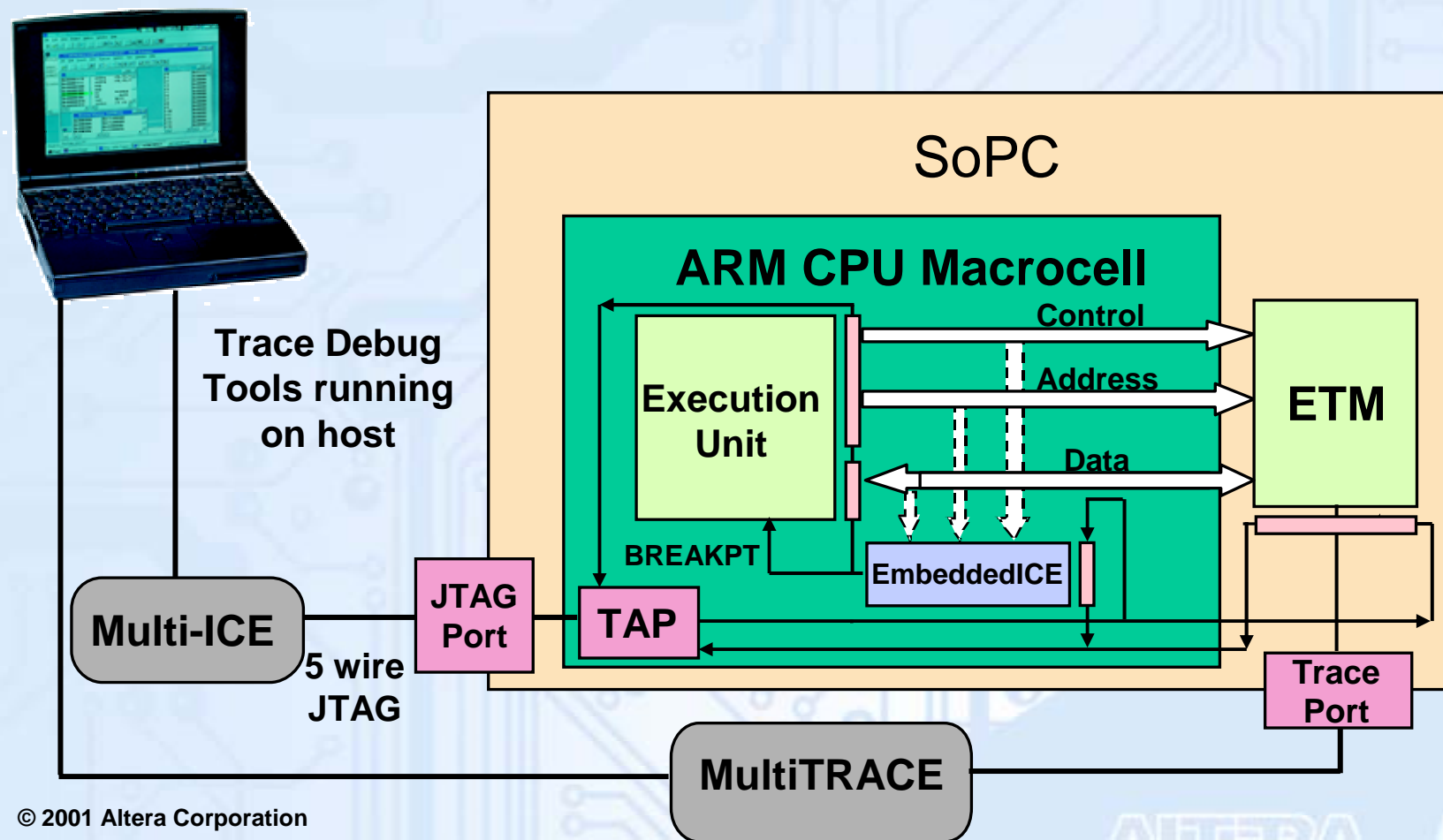
- Supports Excalibur Processors
  - ARM®, Nios™
- Integrated Software Development Environment
- Generate combined programming files
  - PLD configuration plus software code



# ARM Software Development Tools

- Altera provides ARM Developer Suite (ADS lite), comes free with Quartus license.
  - ARMasm (ARM Assembler)
  - Compilers (ARM C/C++ Compiler)
  - ARMLink (ARM linker)
  - AXD – ARM debugger
  - Adwu – ARM debugger for windows/Unix
  - Fromelf – Format Changer (ELF to other formats)
- Altera ADS will be supported with Quartus only
- Full version ADS can be obtained from ARM.
- GNU ARM tools will also be offered by Altera

# ARM Mult-ICE & Multi-Trace Solution



## **ARM-base device RTOS support**

- **VxWorks AE**
- **Nucleus**
- **Linux**
- **Enea OSE**

**RTOS BSP will be provided for our  
Excalibur Development Board**



# EPXA10 Development Board Features

- **Interconnects**
  - 10/100 Ethernet with full and half duplexing
  - 2 PCI connectors
  - Two RS232 ports
- **Memory subsystem**
  - 128Mbyte DDR sited on board for layout issues
  - Up to 512MB SDR SDRAM in a DIMM socket
  - 16MB flash memory
- **Other hardware features**
  - ByteBlaster/MasterBlaster connectors(download, debug, SignalTap)
  - Switches, LEDs, DIP switches
  - EPC2 programming capabilities
- **Clock Flexibility**
  - Crystal on the input clock can be changed
  - External clock generator can be used

## **Excalibur MPLD**

- **Pin-Compatible, Drop-In Replacement for Excalibur Devices**
- **No Extra Effort on Customer Side**
- **Considerable Price Reduction**
- **Timing, I/O and Placement Constraints Are Preserved**
- **4-5 Weeks Prototype Turnaround Time at TSMC, Low NRE**

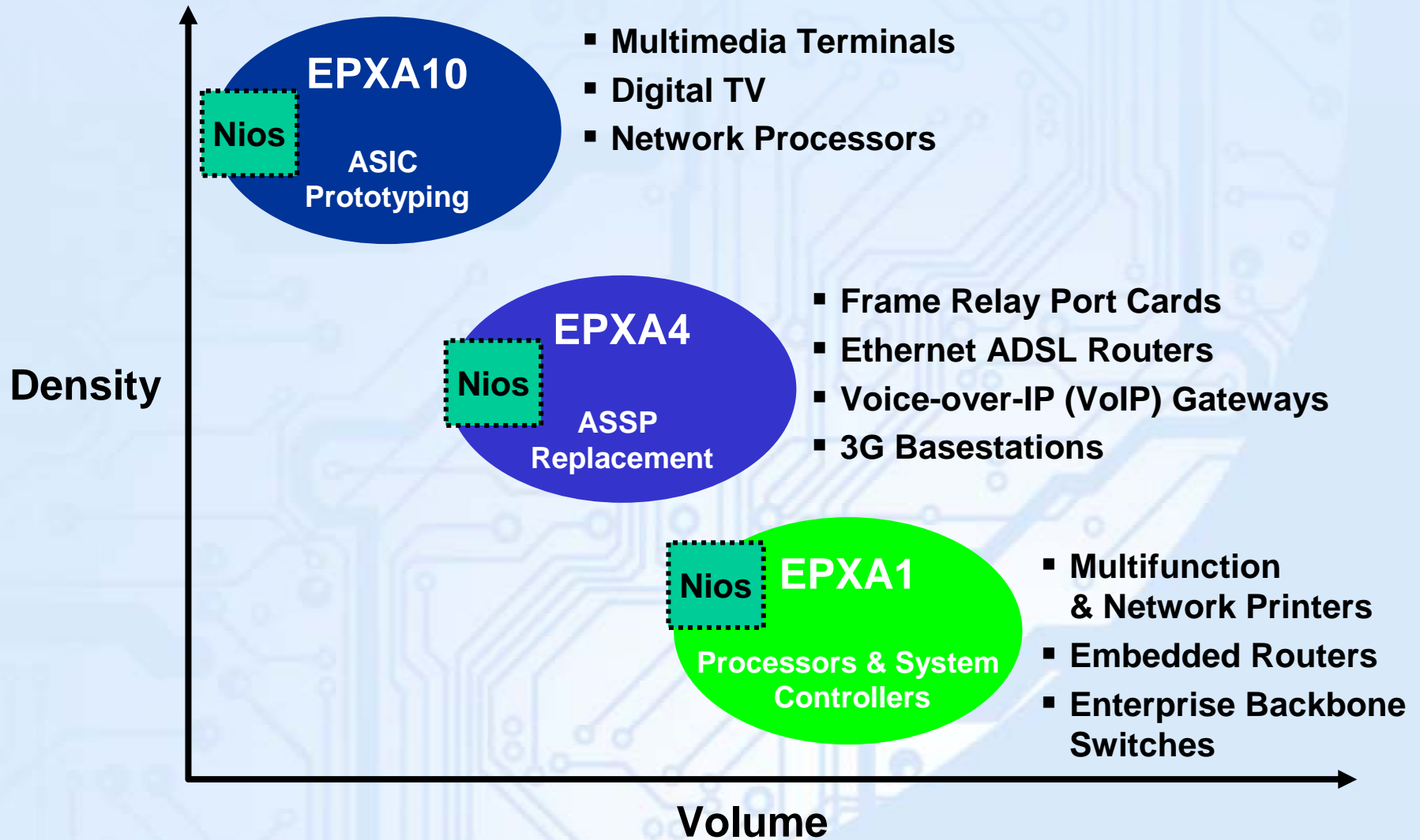
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# **Excalibur ARM-based Devices Application Examples**

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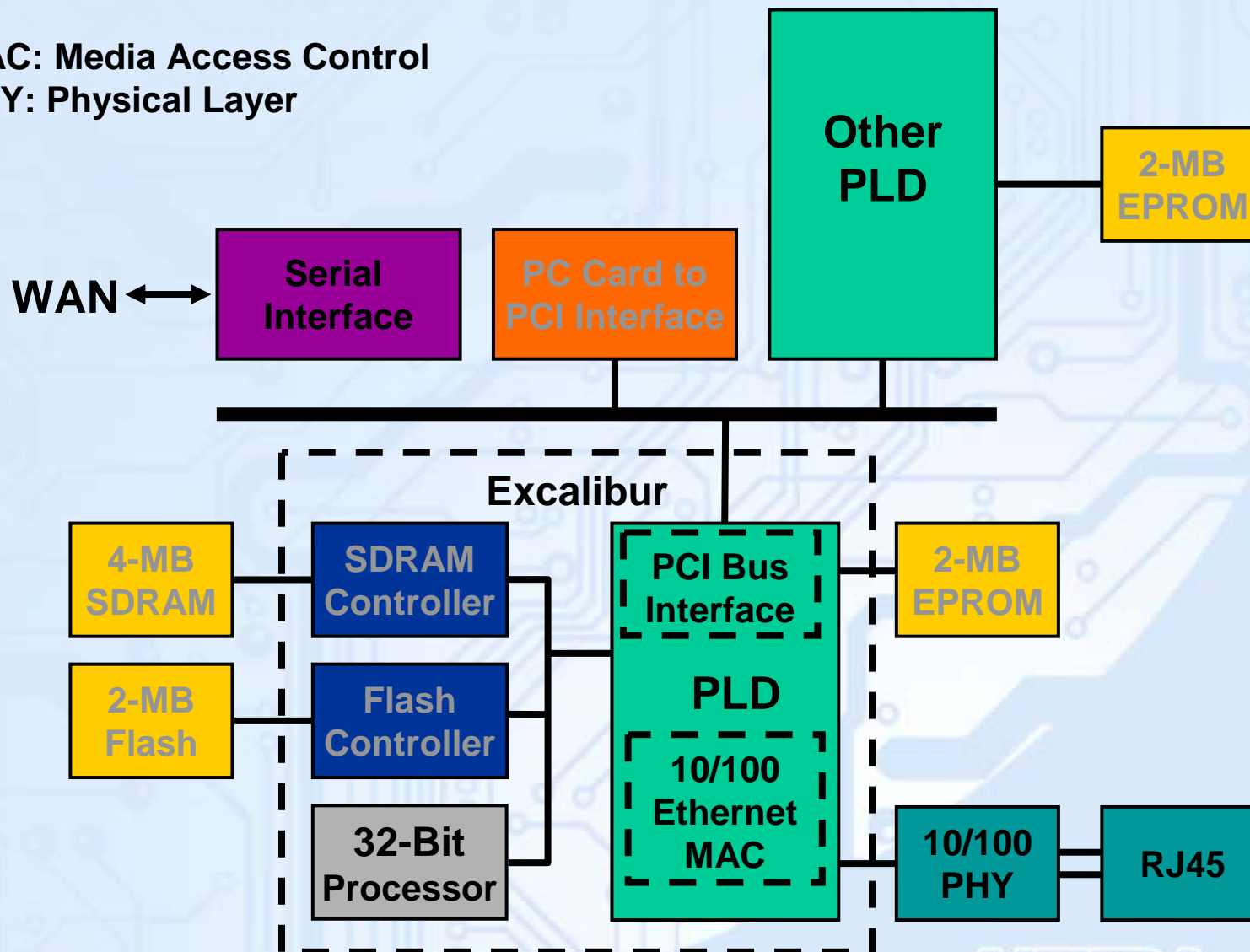
# Excalibur Family Market Fit





# Enterprise Backbone Switches

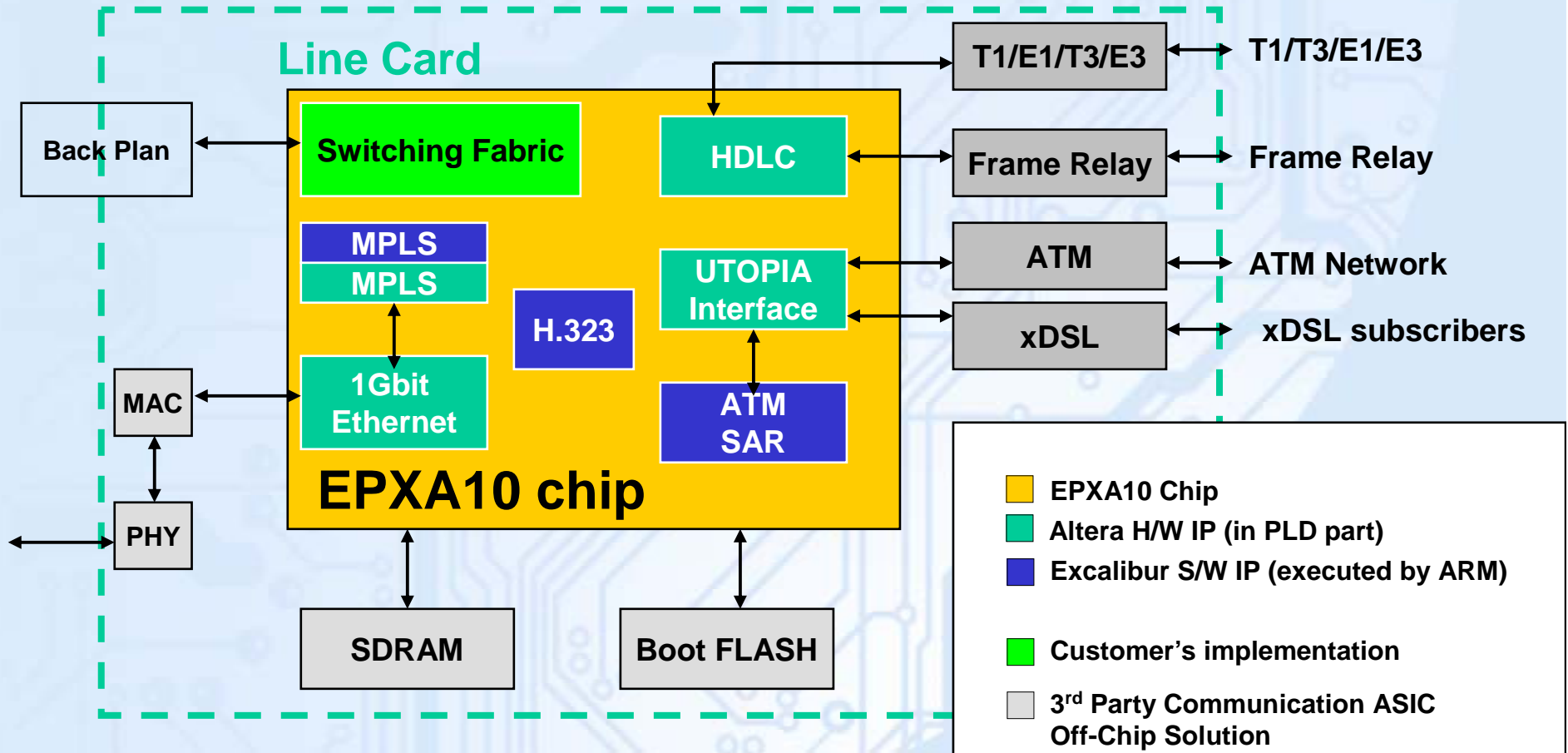
MAC: Media Access Control  
PHY: Physical Layer



# Voice of Packet

## CO Gear Line Card

(Access Multiplexer or Voice Gateway)



# Excalibur ARM-based Device Summary

- **Complete** Solution for SOPC
  - Hardware & Software Solution
  - Development Board, Drivers, IP
  - Built-In Licensing for ARM-based Devices
- **Flexible** Solution
  - Make Changes During Development
  - Make Changes in Production
  - Painless Route to Low-Cost HardCopy Solution
- **Fast** Solution
  - Performance
  - Time-to-Market
  - System Development
    - Quartus II/MegaWizard



*POP QUIZ*

## **Quiz Question**

**Which of the following statement is false?**

- A) Altera provides Excalibur MegaWizard to configure Excalibur embedded stripe.**
- B) Altera provides both bus-functional model & full-stripe model to verify ARM-based Excalibur devices**
- C) Both single-port and dual-port SRAM are part of the embedded stripe of ARM-based Excalibur devices.**
- D) Ethernet MAC and PCI interface are part of the the embedded stripe of ARM-based Excalibur devices.**

## Quiz Answer

Which of the following statement is false?

- A) Altera provides Excalibur MegaWizard to configure Excalibur embedded stripe.
- B) Altera provides both bus-functional model & full-stripe model to verify ARM-based Excalibur devices
- C) Both single-port and dual-port SRAM are part of the embedded stripe of ARM-based Excalibur devices.
- D) Ethernet MAC and PCI interface are part of the the embedded stripe of ARM-based Excalibur devices.