SOPC Test Cores

March 2000, ver. 1

This CD-ROM contains test cores to help developers perform functional tests on their designs.

Test Core Functionality

For implementing a test plan, you can implement multiple cores on an APEX™ device using the JTAG chain and the Quartus™ software. Each core tests one or more interfaces and uses light-emitting diodes (LEDs) to indicate that a design has passed or failed.

Table 1 lists the cores available on this CD-ROM. All of these cores are available in the <*CD-ROM drive*>**:\testcore** directory.

Table 1. Test Cores Available for the Development Board

Test Core Name	Test Interface
Mix_Test_1.sof	Configuration of the APEX device Switches and LED interface VGA interface
Mix_Test_2.sof	SRAM1 interface SRAM2 interface
Mix_Test_3.sof	RS232 interface PS2 interface USB interface Parallel interface PMC interface GPM interface EJTAG interface JTAG chain
Mix_Test_4.sof	FireWire interface Ethernet interface
Mix_Test_5.sof	FLASH interface EPROM interface
Sdram_top.sof	SDRAM interface
Lcd_top.pof **Lcd_top1.pof** **Lcd_top2.pof**	LCD interface EPC2 devices

For more information on the test cores, see the "Testing Software" section in the *System-on-a-Programmable-Chip Development Board User Guide*.