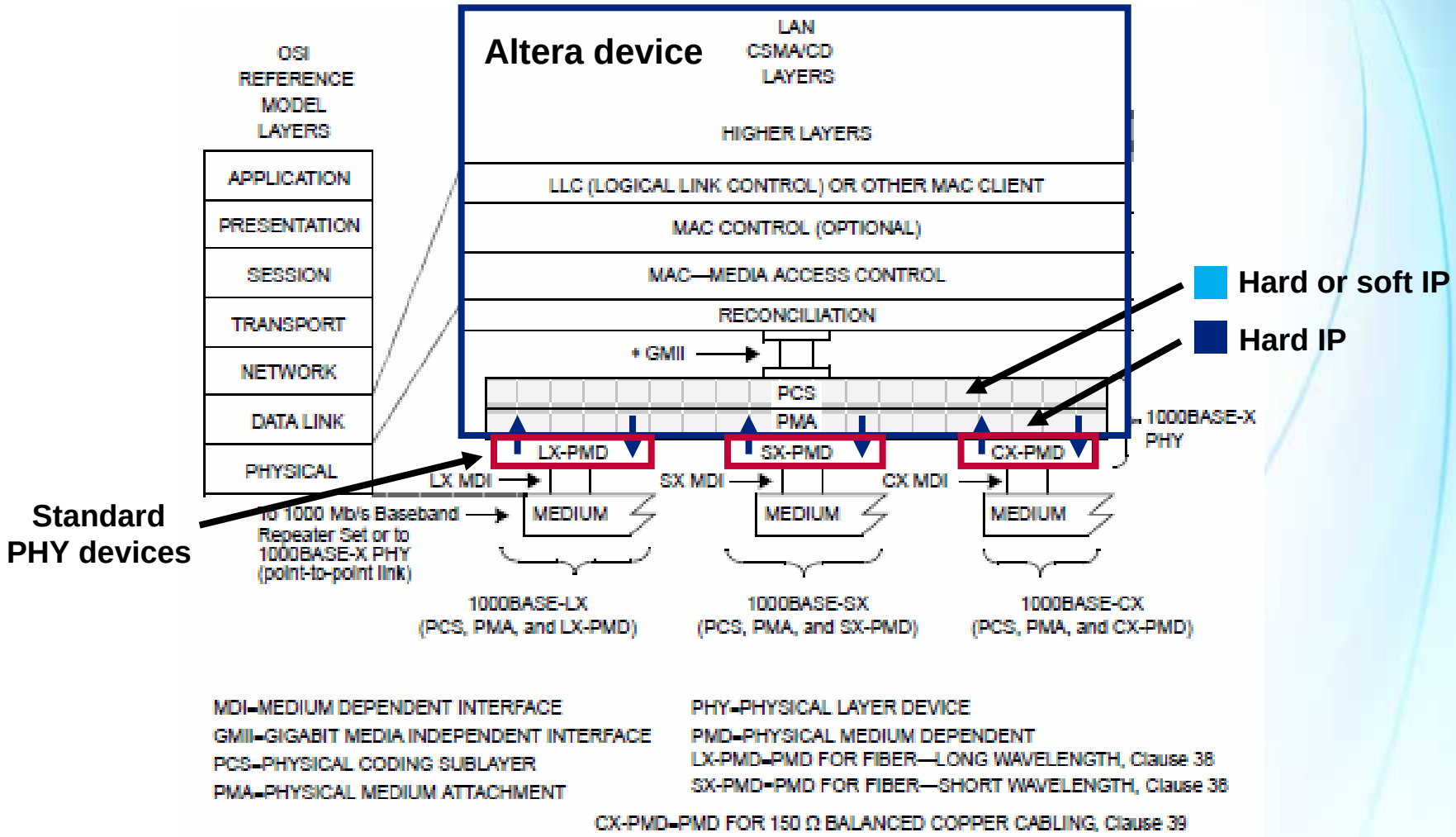
1 Gbps to 10 Gbps Ethernet in Altera Devices

Transceiver Portfolio Workshops 2009

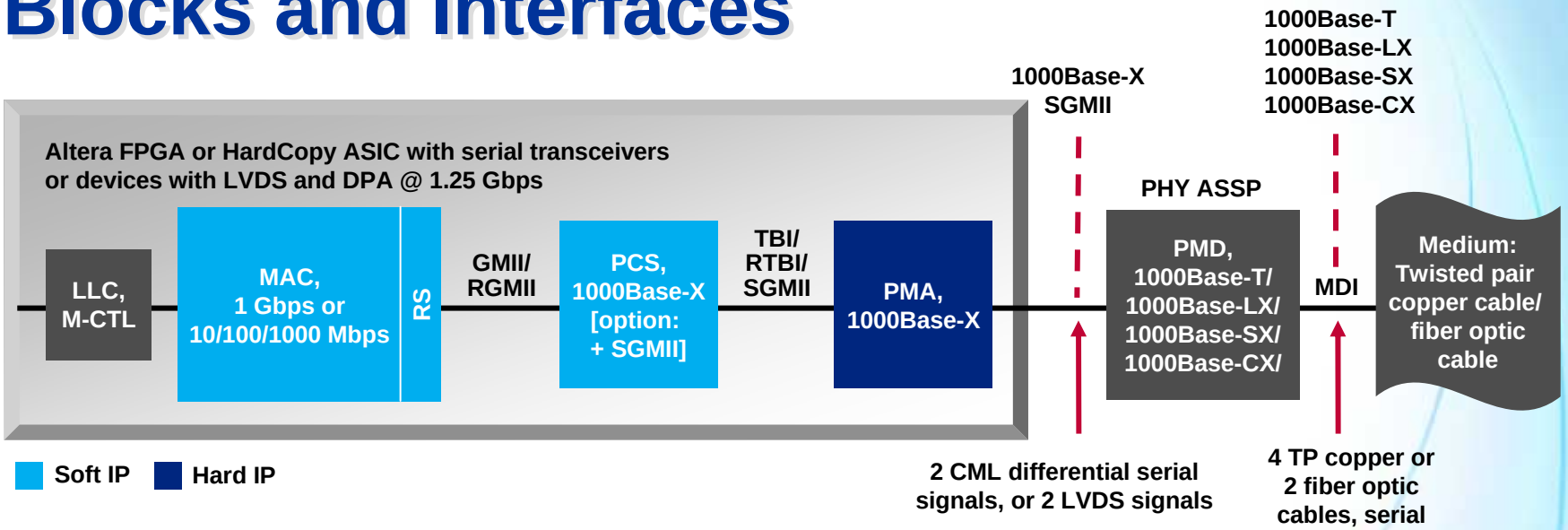
Agenda

- 1 Gbps Ethernet
  - Standards
  - Altera Triple-Speed Ethernet MegaCore, device features, and advantages
  - Standards compliance and validation at Altera
  - Development kit
- 10 Gbps Ethernet
  - Standards
  - Altera 10 GbE IP, device features, and advantages
  - Standards compliance and validation at Altera
  - Development kit

IEEE 802.3 1 Gbps Ethernet Standards Blocks



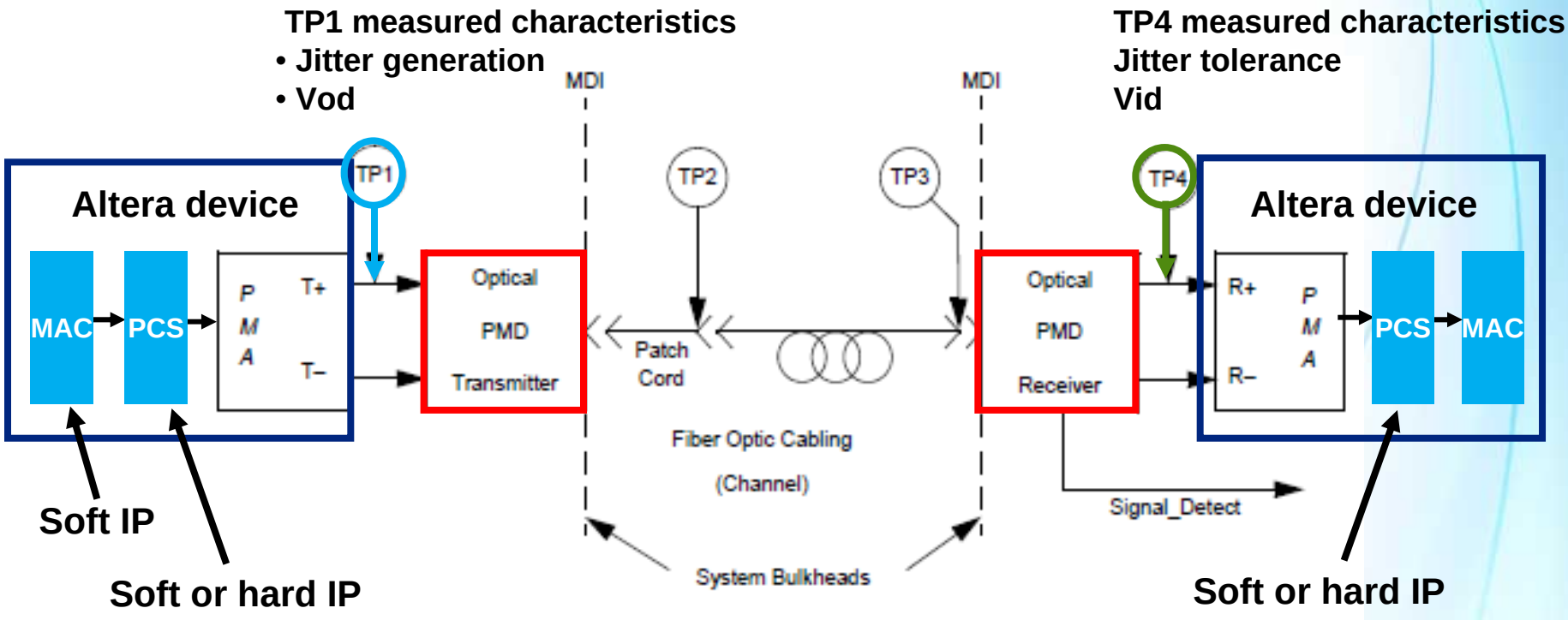
1 Gbps or 10/100/1000 Mbps Ethernet Blocks and Interfaces



- 1000Base-X and SGMII interfaces supported in devices with serial transceivers and in Stratix III and Stratix IV FPGAs, and in HardCopy III and HardCopy IV ASICs with LVDS and soft CDR
- TBI, RTBI, GMII, and RGMII supported in all Cyclone, Stratix, Arria, and HardCopy device families
- Interface
  - GMII: Gigabit media independent interface
  - RGMII: Reduced (pin count) GMII
  - SGMII: Serial GMII
  - TBI: Ten-bit interface
  - RTBI: Reduced (pin count) TBI
  - MDI: Medium dependent interface

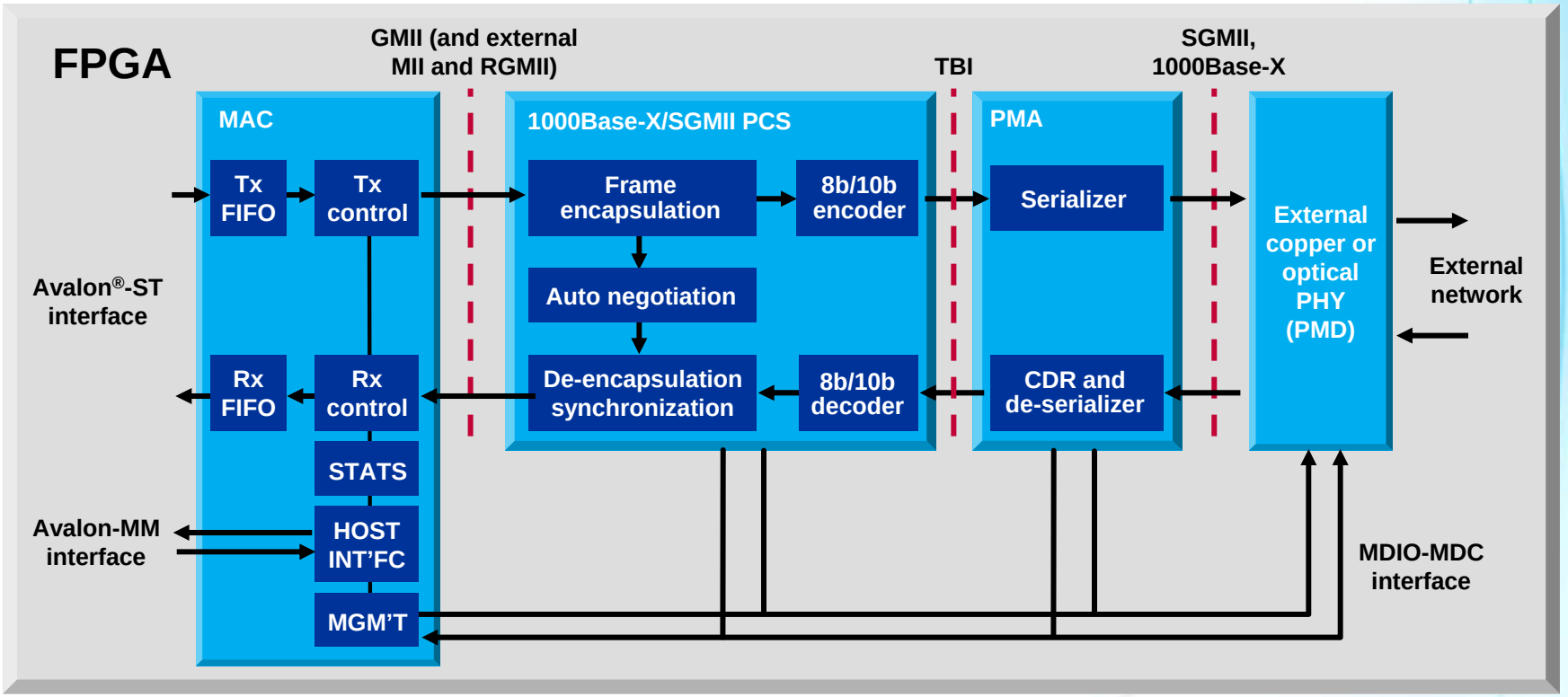
IEEE 802.3 1000Base-X Block Diagram

Key Test Points and Test Criteria



Triple-Speed Ethernet (TSE) MegaCore

- Single to multi-port 10/100 Mbps or 1 Gbps applications
- LAN and WAN data plane or control plane (embedded system) applications
- Chip-to-chip, board-to-board, and inter-system network connectivity



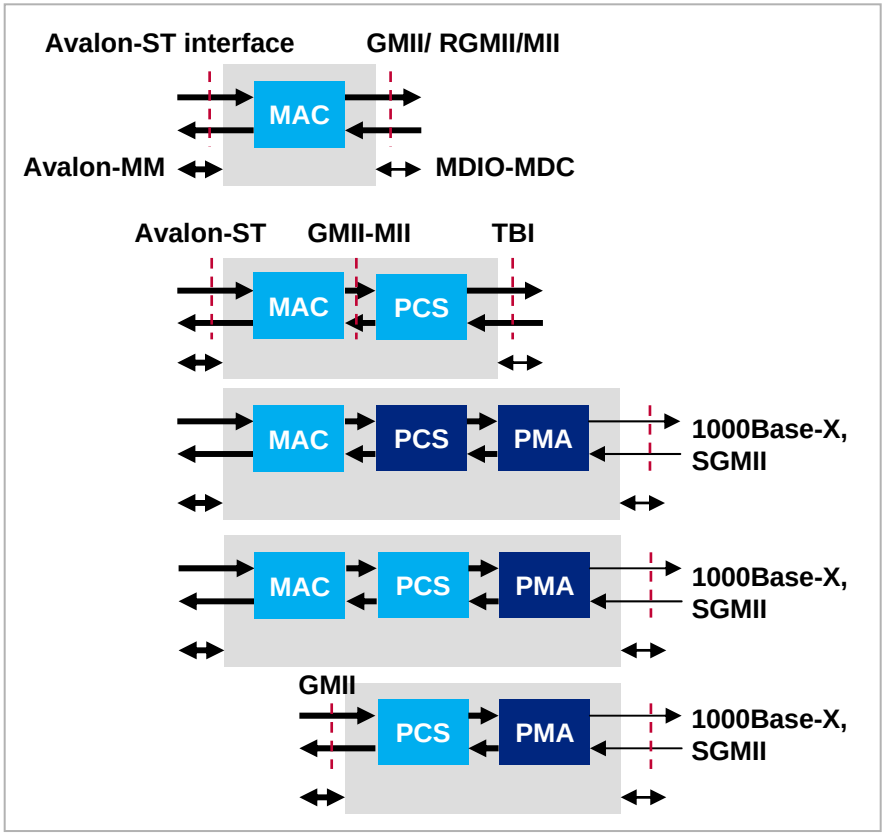
The first and only FPGA with LVDS support for 1 GbE

TSE MegaCore Features

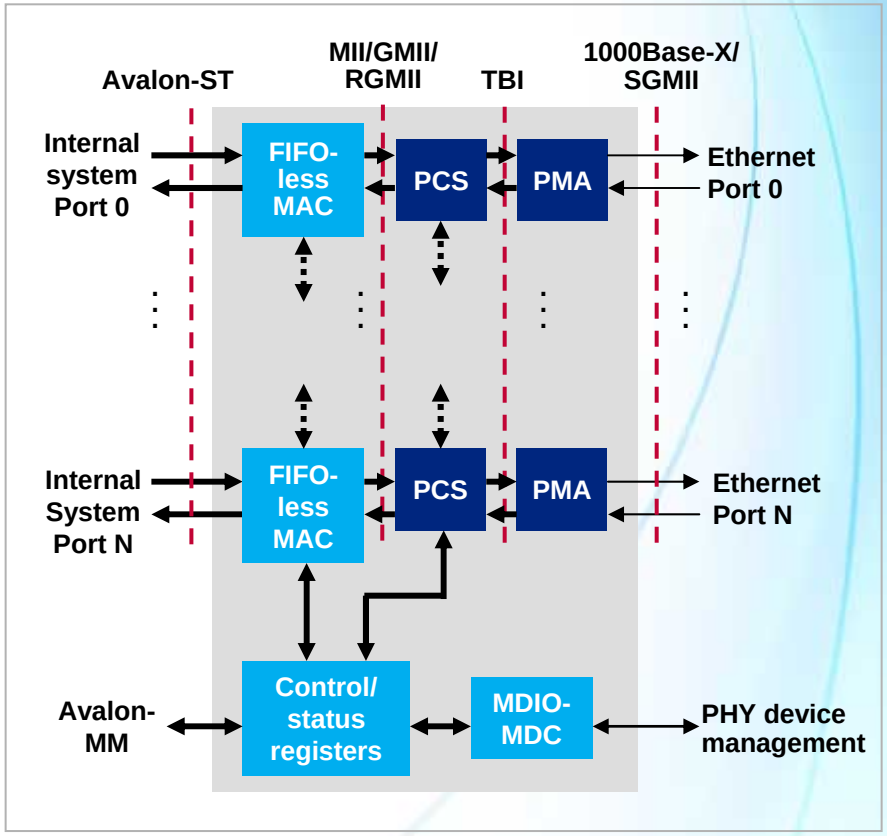
- Half/full-duplex operation in 10/100 Mbps and full duplex in 1-Gbps mode
- Ethernet MAC, PCS, and PMA dynamic configuration to 10/100/1000 Mbps
- IEEE 802.3 standard compliant
- Validated by University of New Hampshire Interoperability Lab (UNH-IOL)
  - Successfully passed the UNH Ethernet tests for 10/100 Mbits and 1 GbE
    - IEEE 802.3 clauses 4 (MAC), 31(flow control), 36 (PCS), 37 (auto-neg.), and interop
- Many supported devices
  - Stratix IV, Arria II GX, Stratix III, Cyclone III, Cyclone II, Stratix II, Stratix II GX, Arria GX, HardCopy III, and HardCopy II devices
- Standard interfaces
  - External Ethernet PHY device: MII, RMII, GMII, RGMII, SGMII, 1000Base-X, and TBI
  - *Supports GbE with SGMII in Stratix IV and Stratix III FPGAs and HardCopy IV and HardCopy III ASICs with LVDS, soft CDR, and a Rx passive equalizer*
    - *The only FPGA with this feature*
    - *Saves many serial transceivers and power for use in other high-speed applications*

TSE MegaCore Configuration Options

Single-port TSE configurations



Multi-port TSE



The only Ethernet multi-port IP core for FPGAs

Soft IP Hard IP

IEEE 802.3 1 GbE PMD Standards and Validation

IEEE 802.3 or industry-standard interface	Cable type and transmission method	IEEE 802.3 clause or other spec.	Signal type	Total jitter (UI)	Deterministic jitter (UI)	Altera characterization on test result
1000Base-CX shielded jumper cable	Two pairs of specialized balanced cabling	Clause 39	CML	TP1 = 0.120 TP4 = 0.710	TP1 = 0.120 TP4 = 0.450	✓
SGMII (10/100/1000 Mbps)	Two pairs of signal traces on boards and backplanes	Cisco SGMII spec	LVDS	TP1 = 0.240 TP4 = 0.710	TP1 = 0.120 TP4 = 0.450	✓ LVDS char.
SFP pluggable module	Optical or copper	SFP spec 2000	100 OHM Diff. AC-coupled Vrx out(Diff) = 370-2000 mV, Vrx (S.E)= 185-1000mV, Vtx input (diff) = 500-1200mV, Vtx (S.E.) = 250-600mV	Optical TP1 = 0.240 TP4 = 0.749 Copper TP1 = 0.240 TP4 = 0.710	Optical TP1 = 0.100 TP4 = 0.462 Copper TP1 = 0.120 TP4 = 0.450	✓ LVDS char.
1000Base-SX short wavelength optical	Full-duplex multi-mode fibers	Clause 38	Optical to network, CML or LVDS to FPGA	TP1 = 0.240 TP4 = 0.749	TP1 = 0.100 TP4 = 0.462	✓
1000Base-LX long wavelength optical	Duplex single-module fibers or duplex multi-mode fibers	Clause 38	Optical to network CML or LVDS to FPGA	TP1 = 0.240 TP4 = 0.749	TP1 = 0.100 TP4 = 0.462	✓
1000Base-T category 5 UTP	Advanced multi-level signaling over 4 pairs of Cat-5 balanced un-shielded twisted pair copper cables	Clause 40	4D PAM5	--	--	--

10/100/1000 Mbps Ethernet MAC, PCS Standards, and Validation

IEEE 802.3 or industry standard interface	IEEE 802.3 clause or spec.	Altera automated verification in each Quartus software release	Altera hardware tests in each Quartus software release	UNH validation test passed
MAC at 10/100 Mbps and 1 Gbps	Clause 4	✓	✓	✓ Stratix II FPGA in Q4-2007 ■ Stratix IV GX and Arria II GX tests to be performed in 2009
MAC MII/GMII interfaces	Clause 35	✓	✓	--
MAC flow control	Clause 31	✓	✓	✓ Stratix II FPGA in Q4-2007 ■ Stratix IV GX and Arria II GX tests in 2009
1000Base-X PCS	Clause 36	✓	✓	✓ Stratix II GX FPGA with soft PCS IP in Q4-2007 ✓ Stratix II GX FPGA with hard PCS IP with SERDES in GbE mode in Q1-2008 ■ Stratix IV GX and Arria II GX tests in 2009
1000Base-X PCS auto-negotiation	Clause 37	✓	✓	✓ Stratix II GX FPGA with soft PCS IP in Q4-2007 ✓ Stratix II GX FPGA with hard PCS IP with SERDES in GbE mode in Q1-2008 ■ Stratix IV GX and Arria II GX tests in 2009
SGMII PCS (10/100/ 1000 Mbps)	Clause 36 and Cisco SGMII spec	✓	✓	✓ Stratix II GX FPGA with soft PCS IP in Q4-2007 ✓ Stratix II GX FPGA with hard PCS IP with SERDES in GbE mode in Q1-2008 ■ Stratix IV GX and Arria II GX tests in 2009
1000Base-T PCS	Clause 40	N/A, no integrated 1000Base-T PHY in Altera devices	N/A	N/A
10/100 Mbps PCS	Other clauses	Not supported by Altera IP, but SGMII PCS supports 10/100 Mbps rates	--	--

TSE Validation

- Stratix II GX verification
  - PCI Express Development Kit, Stratix II GX Edition
  - UNH (University of New Hampshire) test suites based on IEEE 802.3 Ethernet standard (MAC, PCS, and 1000Base-X PMA) passed
  - Device characterization showed compliance with 1000Base-X PMA
- Stratix II verification
  - GbE and 10/100 fast Ethernet verification
  - Nios II Development Kit, Stratix II Edition with Marvell 10/100/1000 88E1111 PHY daughtercard
  - UNH test suites (MAC) passed
- SGMII
  - Serial CDR/SERDES implementation, Rx and Tx identical to 1000Base-X
  - Stratix II GX SERDES and Stratix III LVDS characterization showed SGMII compliance

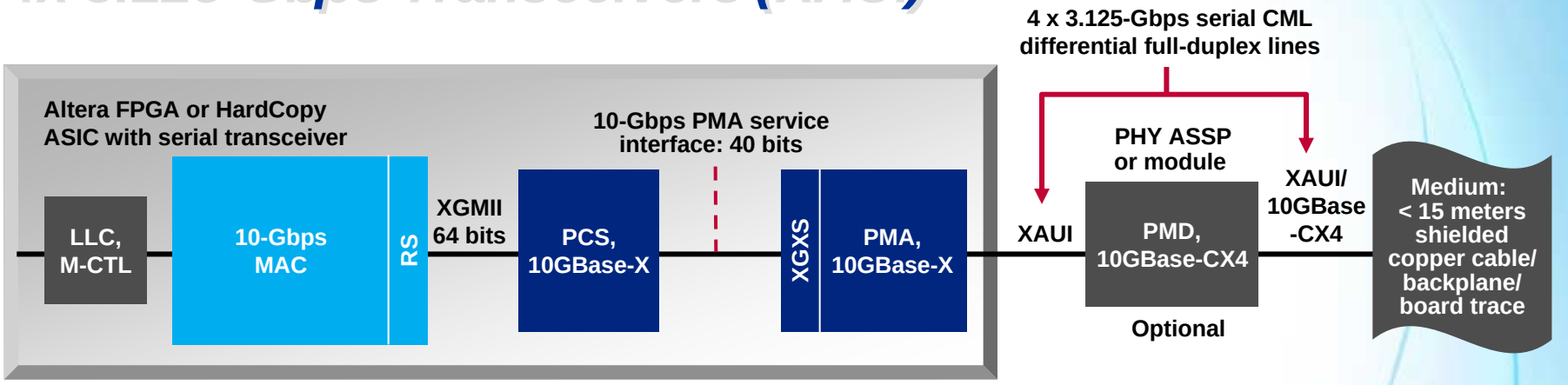
Hardware Verification

MegaCore configuration for interoperability	Interoperability hardware platform		
	Development kit	SERDES Ethernet 10/100/1000 PHY	SFP module
MAC plus 1000Base-X PCS interoperability with copper/optical Gigabit SFPs	Nios II Development Kit, Stratix II Edition	Texas instruments TLK2201 PHY on Optiworkx MoreThanIP daughtercard	Stratos SPLC-20-4-X-SL (optical Gigabit)
			Finisar FCMJ-8521-3 (copper Gigabit)
MAC plus 1000Base-X PCS plus PMA interoperability with copper/optical Gigabit SFPs	PCI Express Development Kit, Stratix II GX Edition	Stratix II GX embedded transceiver	Stratos SPLC-20-4-X-SL (optical Gigabit)
			Finisar FCMJ-8521-3 (copper Gigabit)
MAC plus 1000BaseX-PCS-SGMII interoperability with copper SFPs	Nios II Development Kit, Stratix II Edition	Texas instruments TLK2201 PHY on Optiworkx MoreThanIP daughtercard	Finisar FCMJ-8521-3 (copper Gigabit)
MAC plus 1000BaseX-PCS-SGMII plus PMA interoperability with copper SFPs	PCI Express Development Kit, Stratix II GX Edition	Stratix II GX embedded transceiver	Finisar FCMJ-8521-3 (copper Gigabit)

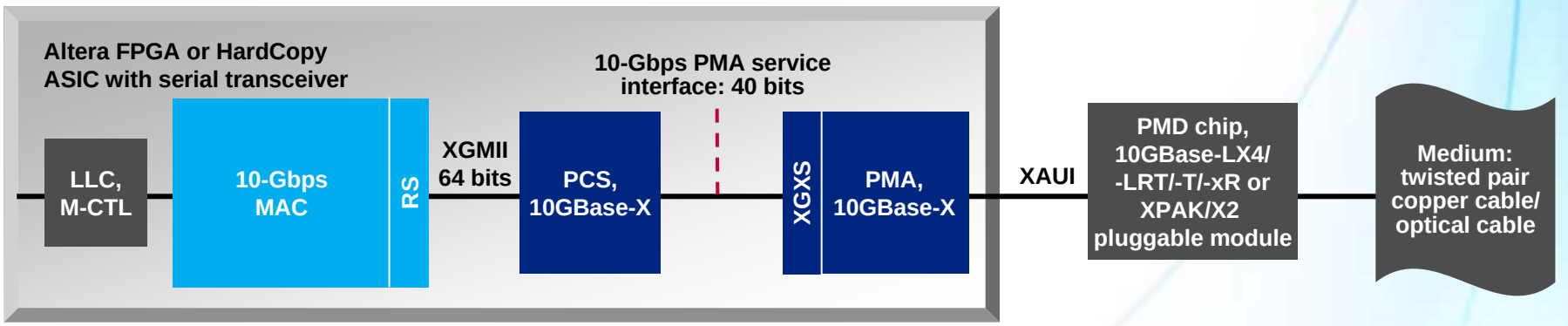
10 Gbps Ethernet

10 GbE Standard Blocks and Interfaces

4x 3.125-Gbps Transceivers (XAUI)



MAC and 10GBase-X (8B/10B) PHY in backplane and LAN applications

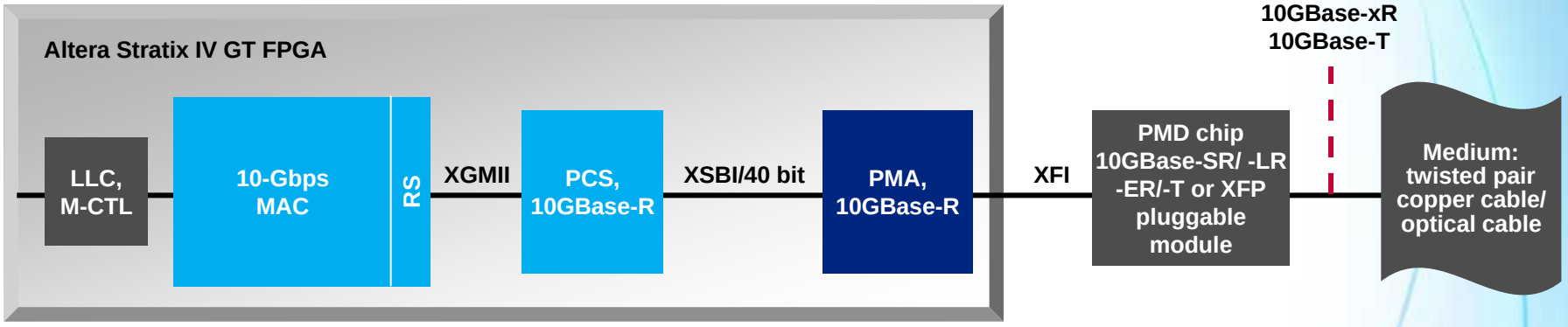


MAC and 10GBase-X PHY in LAN, or WAN (-R in PHY device) applications

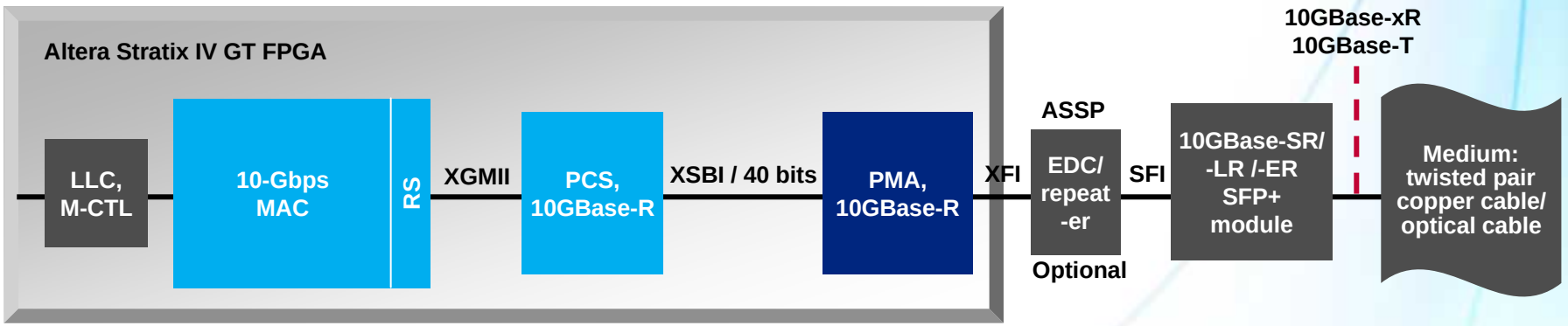
Soft IP **Hard IP**

10 GbE Standard Blocks and Interfaces

10-Gbps Transceiver



XFP and 10GBase-R (64b/66b) PHY, low I/O count and cost solution



SFP+ and 10GBase-R (64b/66b) PHY, low I/O count, cost and power solution

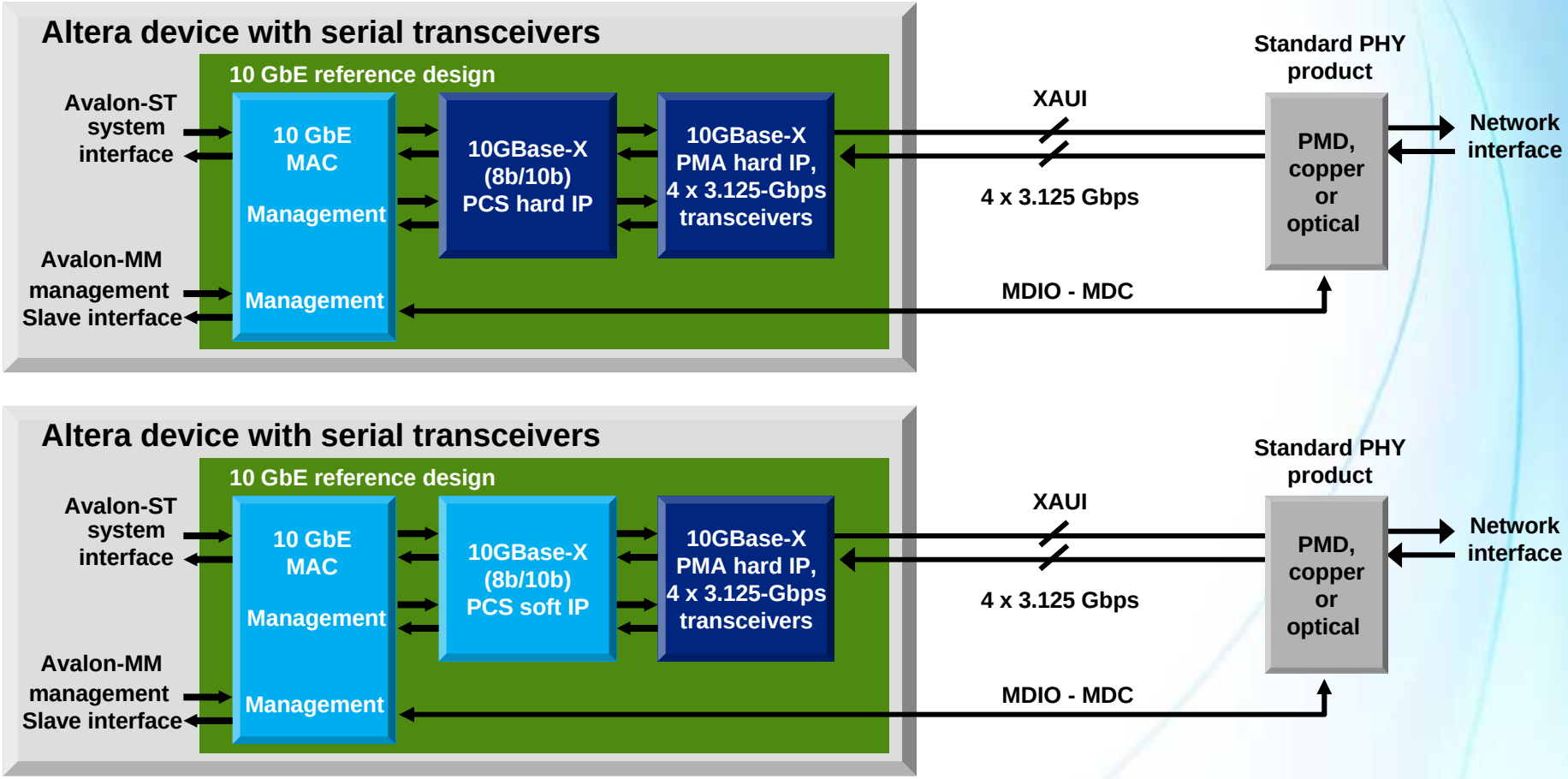
Soft IP **Hard IP**

Altera 10 GbE IP Features

- Full-duplex operation supporting Ethernet 10-Gbps data rate
- IEEE 802.3ae 2002 10 GbE standards compliant
- Validated by UNH in Stratix II GX FPGA
- Easy MegaWizard™ user configuration software
- SOPC Builder compliant
- Many supported devices:
  - Stratix IV (GX, GT, and E), Stratix III, Stratix II, Stratix II GX, Arria GX, Arria II GX, and HardCopy III device families
- Competing 10 GbE IP uses 1,200 more LUTs just for XAUI logic, and:
  - Does not have system side Tx and Rx FIFOs
  - Does not have local and line loopback
  - Does not have receive frame filtering

10 GbE Reference Design

XAUI Interface

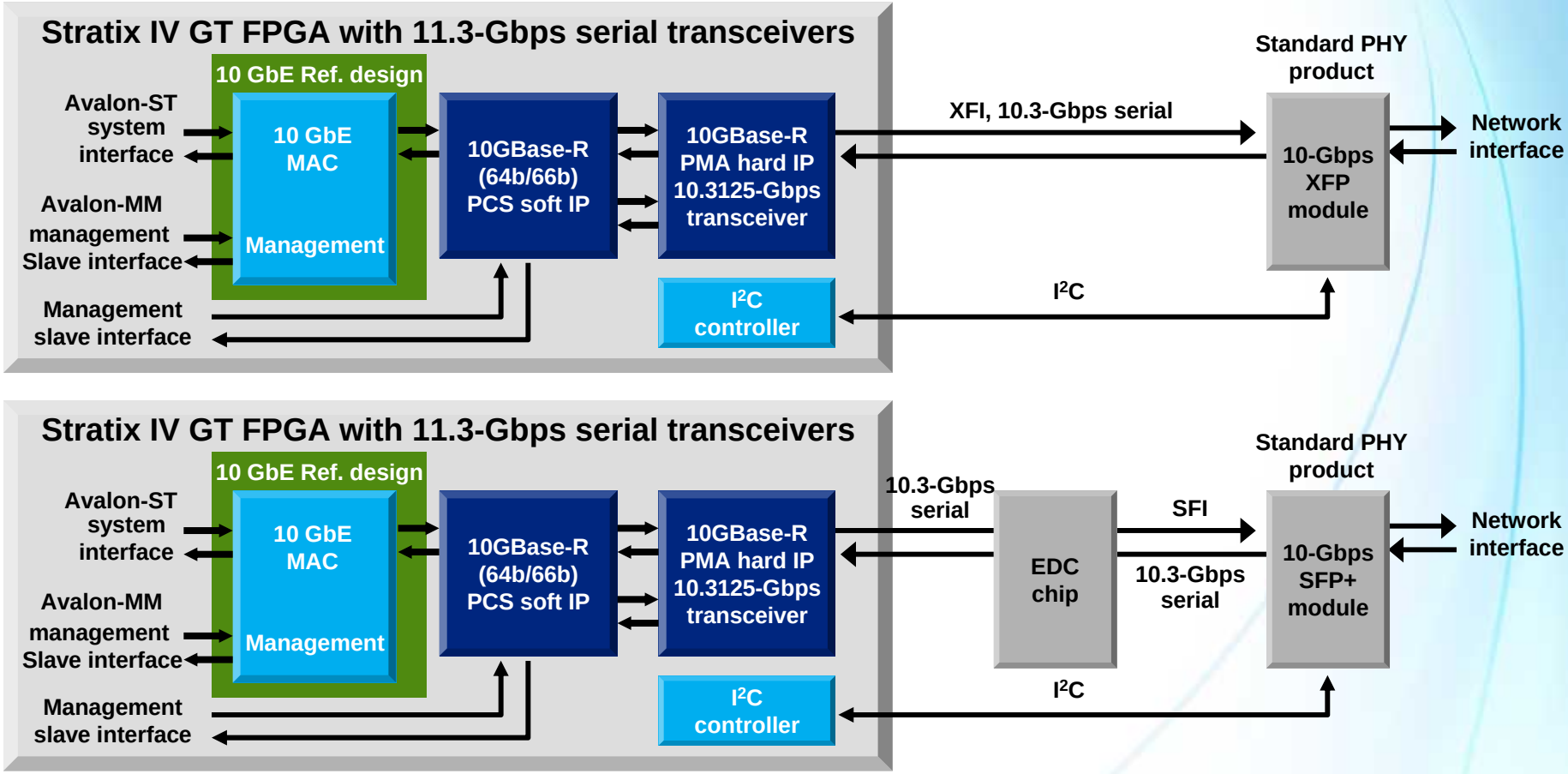


- Soft PCS: for utilization of transceiver block CMU channels in XAUI

Soft IP **Hard IP**

10 GbE Reference Design

XFI and SFI 10.3-Gbps Interfaces: Lowest Power and Lowest System Cost



The first and only 10Gb serial based Ethernet solution in FPGAs

Note:Some system channels may not need EDC chip.
10GBase-R PCS IP available from MoreThanIP.

10 GbE Validation

- 10 GbE MAC and PCS verification
- Hardware validation of MAC, PCS, and PMA
  - Tested by Altera with Altera Stratix II GX PCIe development kit with XAUI interface
    - With CX4 adapter and 10 GbE switch and Spirent Communications 10 GbE test equipment
    - With X2 optical modules (Finisar and Opnext) to Spirent Communications 10 GbE test equipment
  - UNH tested with Stratix II GX FPGA
    - With PCIe development kit and CX4 for MAC and PCS tests (IEEE 802.3ae standard clauses 4, 31, 46, and 48)
    - With signal integrity (SI) development kit for XAUI PMA (PMD) tests (IEEE 802.3ae standard clause 47)

IEEE 802.3 10 GbE PMD Standards and Validation

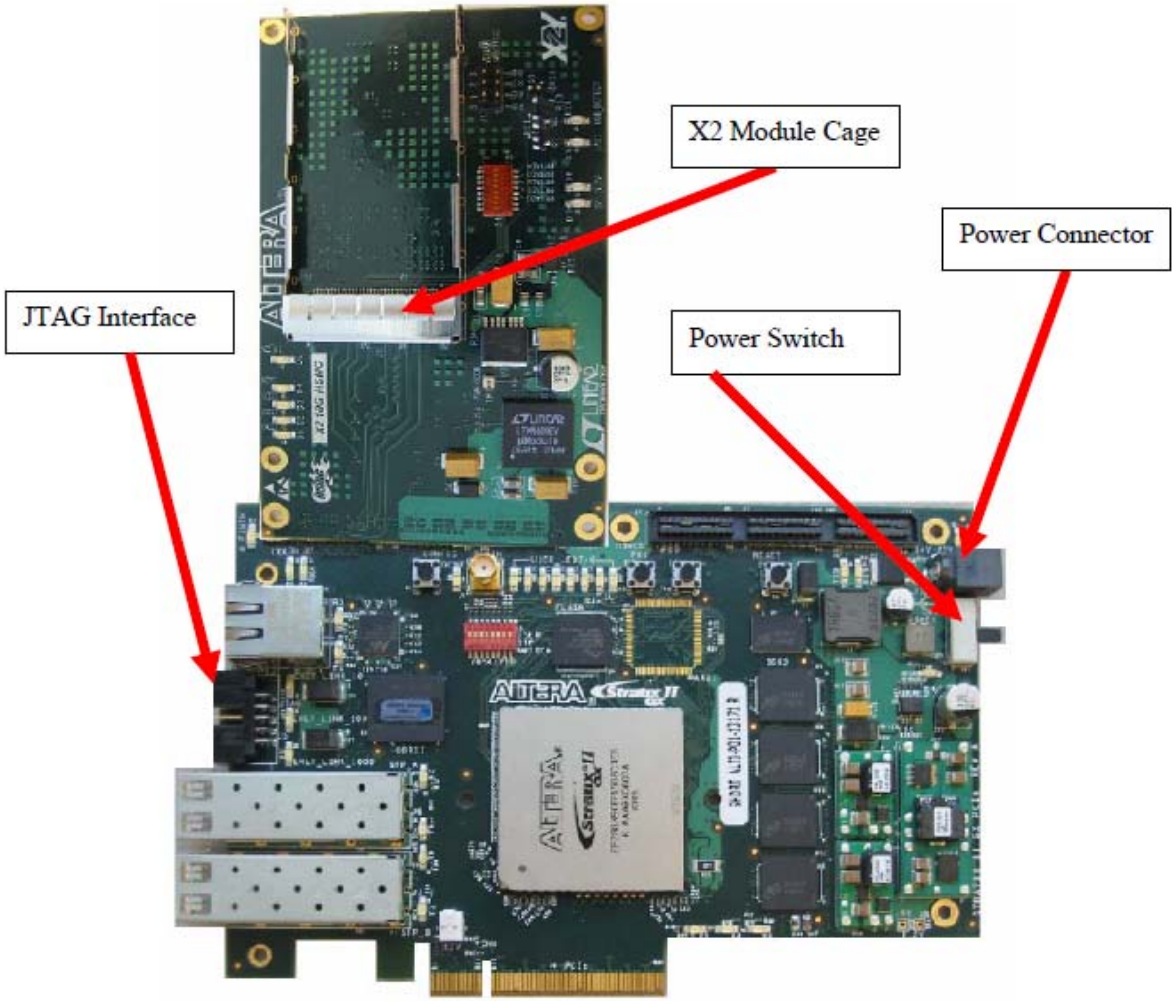
IEEE 802.3 or industry-standard interface	Cable type and transmission method	IEEE 802.3 clause or other spec.	Signal type and Baud rate per serial lane	Altera characterization or other test results
XAUI	4 pairs of copper signal traces on board up to 50 cm	Clause 47	CML, 3.125 Gbps	✓ Stratix II GX Altera characterization tests in 2006 ✓ UNH XAUI validation with Stratix II GX FPGA in Aug. 2008 ✓ UNH XAUI interop tests with Stratix II GX FPGA in Aug. 2008 ■ Stratix IV GX and Arria II GX tests to be done in 2009
X2 pluggable module	FPGA side: XAUI, 4 pairs of copper signal traces on board up to 50 cm	X2 MSA 2005, clause 47	FPGA side: CML, 3.125 Gbps	✓ Stratix II GX Altera internal tests in 2006 ✓ UNH X2 pluggable module validation with Stratix II GX FPGA in Aug. 2008 ■ Stratix IV GX and Arria II GX tests to be done in 2009
XFI for XFP pluggable module	FPGA side: 2 pairs of copper signal traces on board, 8 inches	SFF INF-8077i, 2005, Chapter 3	CML, 10.3125 Gbps	■ Stratix IV GT Altera characterization tests to be done in 2009 ■ UNH XFP module validation with Stratix IV GT FPGA in 2009
SFI for SFP+ pluggable module	FPGA side: 2 pairs of copper signal traces on board, 8 inches	SFF 8431, 2007, Chapter 3	CML, 10.3125 Gbps	■ Stratix IV GT Altera characterization tests to be done in 2009 ■ UNH XFP module validation with Stratix IV GT FPGA in 2009
10GBase-CX4	8 pairs of copper cable	Clause 54	CML, 3.125 Gbps	■ No Altera characterization ■ UNH tests with Stratix II GX FPGA done in Aug. 2008
10GBase-SR, LR, ER, SW, LW, EW	A pair of signal mode or multi-mode fiber	Clause 52	Optical, 10.3125 Gbps	N/A
10GBase-LX4	4 pairs of multi-mode fiber	Clause 53	Optical, 3.125 Gbps	N/A
10GBase-T	4 pairs of copper cable	Clause 54	PAM 16,800 Mbps	N/A. no integrated 10GBase-T PHY in Altera device

10 GbE MAC, PCS Standards, and Validation

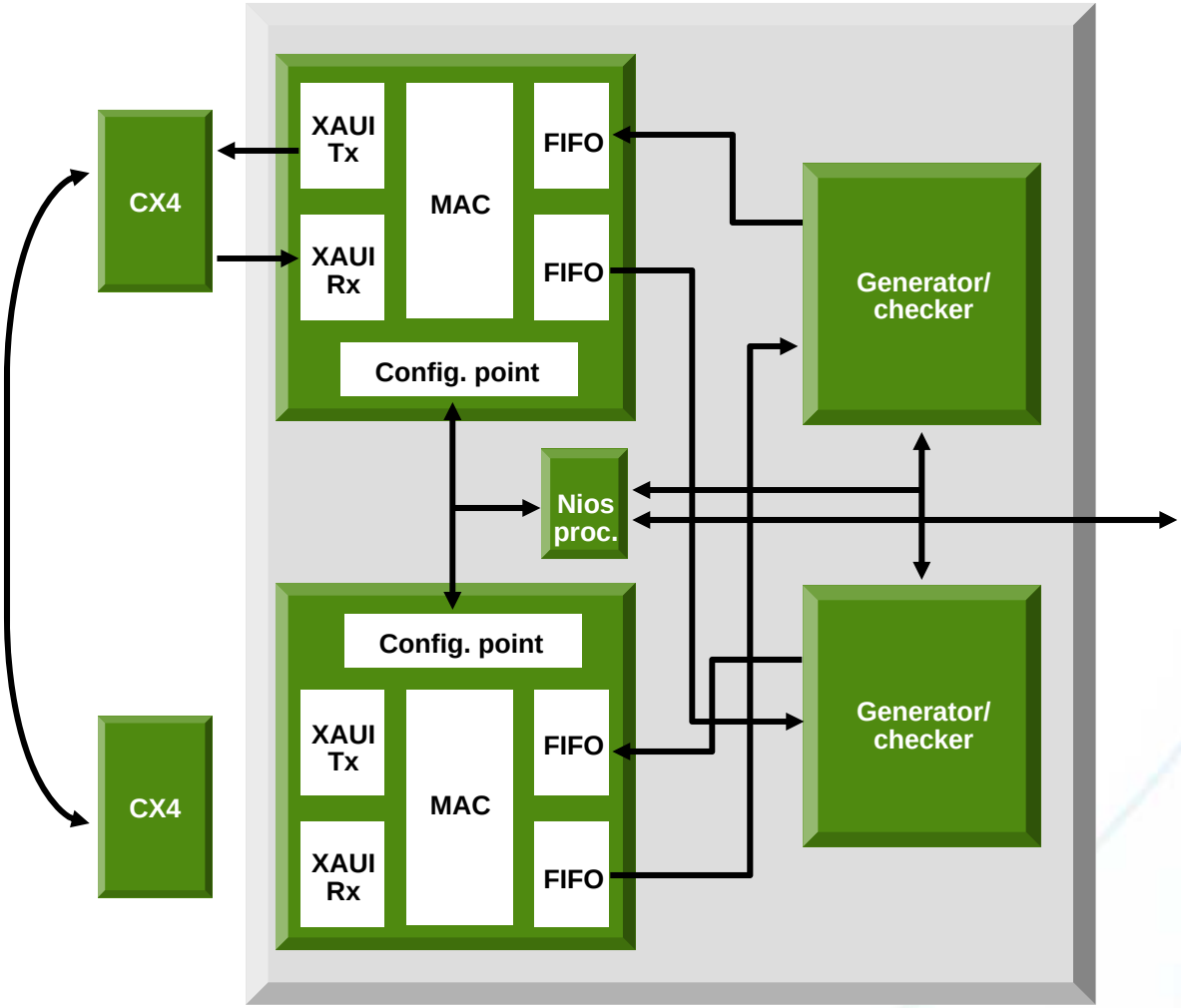
IEEE 802.3 or industry standard interface	IEEE 802.3 clause or spec.	Altera automated verification in each Quartus software release	Altera hardware tests in each Quartus software release	UNH validation test passed
MAC, 10 Gbps	Clause 4	✓	✓	✓ Stratix II GX FPGA (with PCIe dev kit and CX4 adapter card) in June 2008 ■ Stratix IV GX and Arria II GX test to be performed in 2009
RS, 20 Gbps (XGMII interface)	Clause 46	✓	✓	✓ Stratix II GX FPGA (with PCIe dev kit and CX4 adapter card) in June 2008 ■ Stratix IV GX and Arria II GX test to be performed in 2009
MAC flow control	Clause 31	✓	✓	✓ Stratix II GX FPGA (with PCIe dev kit and CX4 adapter card) in June 2008 ■ Stratix IV GX and Arria II GX tests in 2009
10GBase-X PCS	Clause 48	✓	✓	✓ Stratix II GX FPGA with hard PCS IP (with PCIe dev kit and CX4) July 2008 ■ Stratix IV GX and Arria II GX tests in 2009
10GBase-X PCS	Clause 48	✓	✓	■ Stratix II GX FPGA with soft PCS IP (with PCIe dev kit and CX4) to be performed in 2009 ■ Stratix IV GX and Arria II GX tests in 2009
10GBase-R PCS	Clause 49	--	--	Stratix IV GT tests in 2009
10GBase-w, WIS	Clause 50	--	--	--
10GBase-T PCS	Clause 55	N/A, no integrated 10GBase-T PHY in Altera devices	N/A	N/A

Hardware Demo and Test Platform

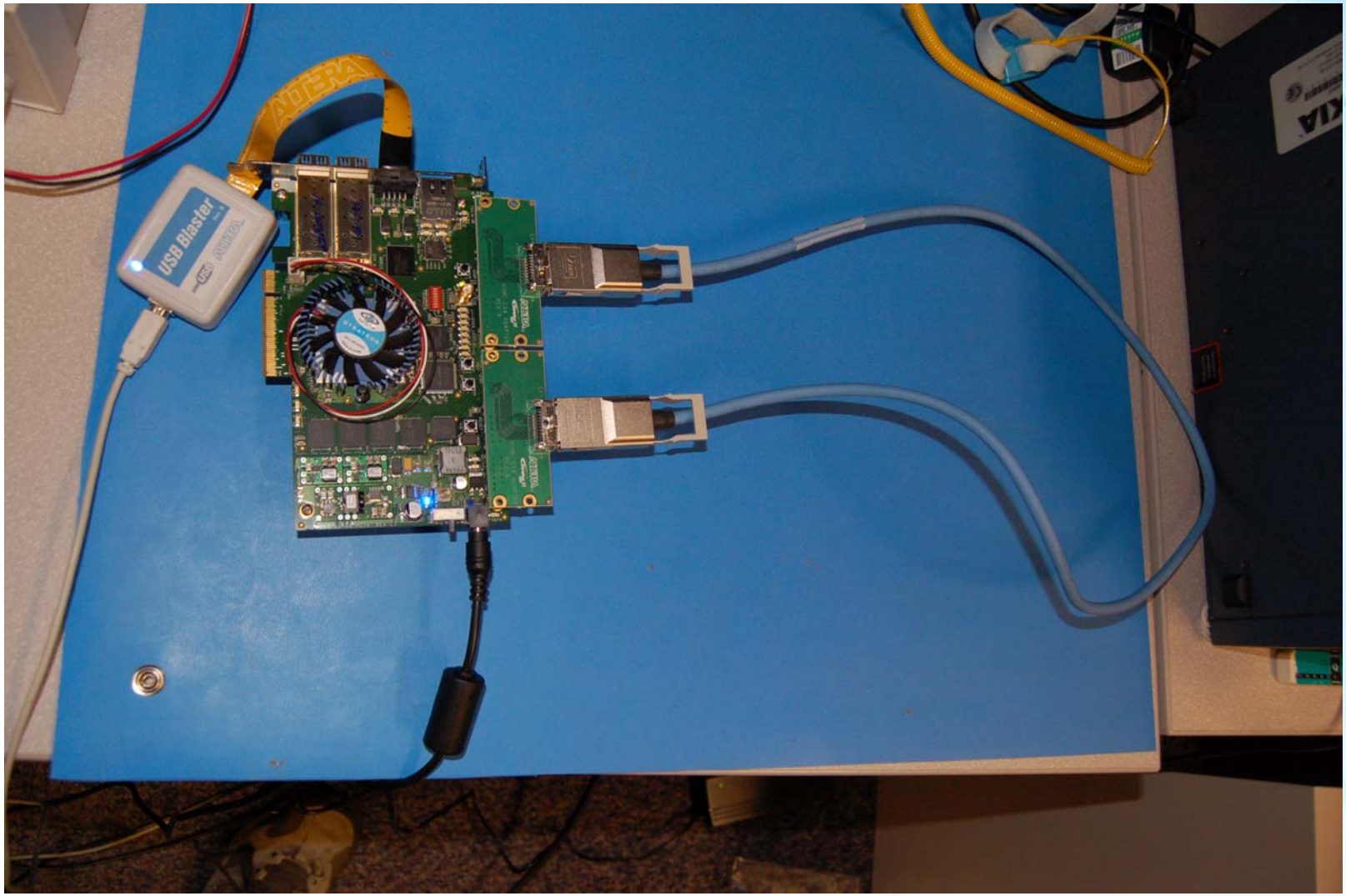
Stratix II GX PCIe Dev Kit and X2 Module Card



Hardware Demo and Test Platform – Reference Design in Stratix II GX PCIe Dev Kit (EP2SGX130 for 2 XAUI Ports)



Hardware Demo



Hardware Demo

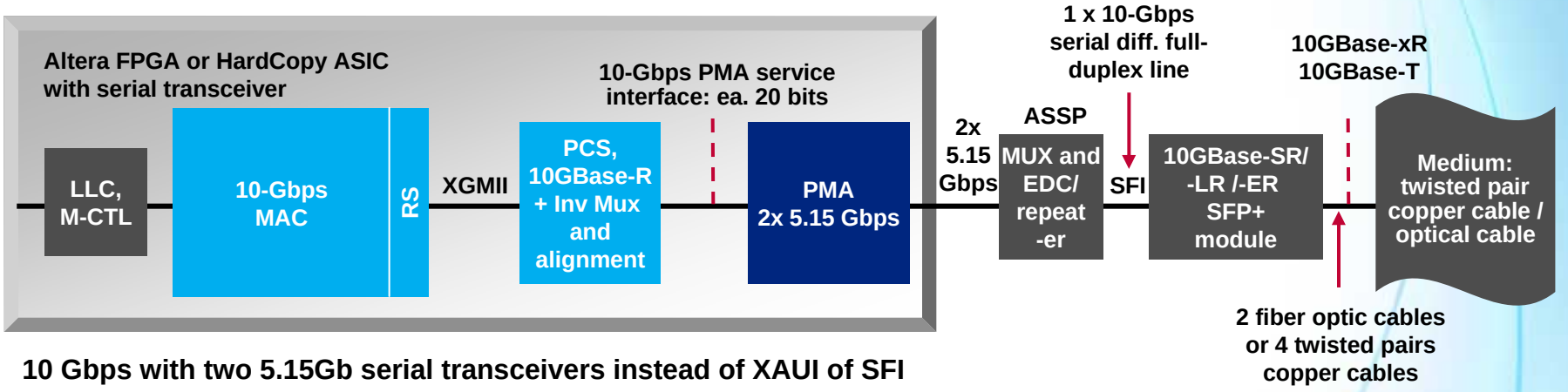
- PC-controlled Nios II soft processor
- Uses loop-back module for data transfer
- Requests some data generation
- Checks data received
- Checks performance

Available now for customer demo

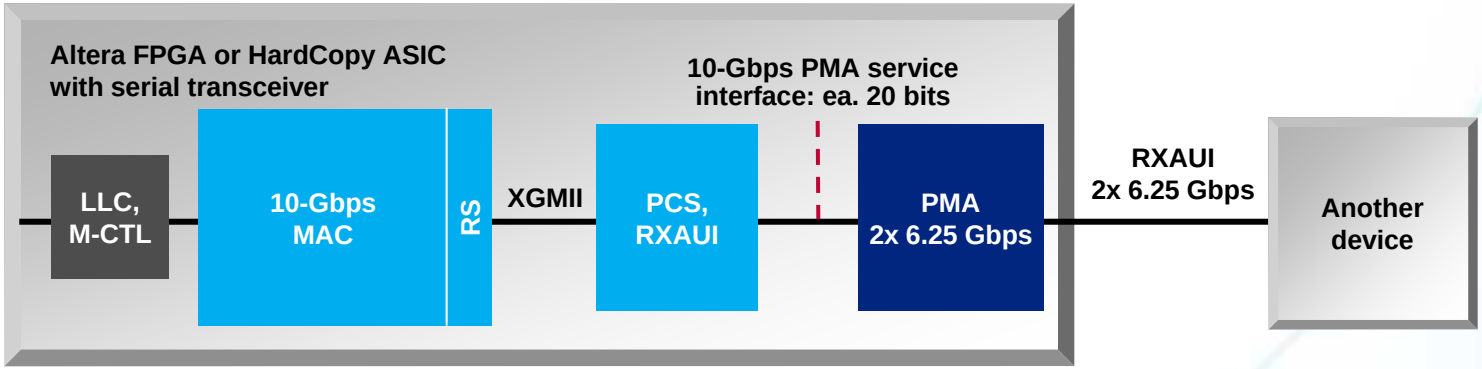
Thank You

10 GbE Blocks and Interfaces

2x 5.15-Gbps or 2x 6.25-Gbps Transceivers



10 Gbps with two 5.15Gb serial transceivers instead of XAUI of SFI

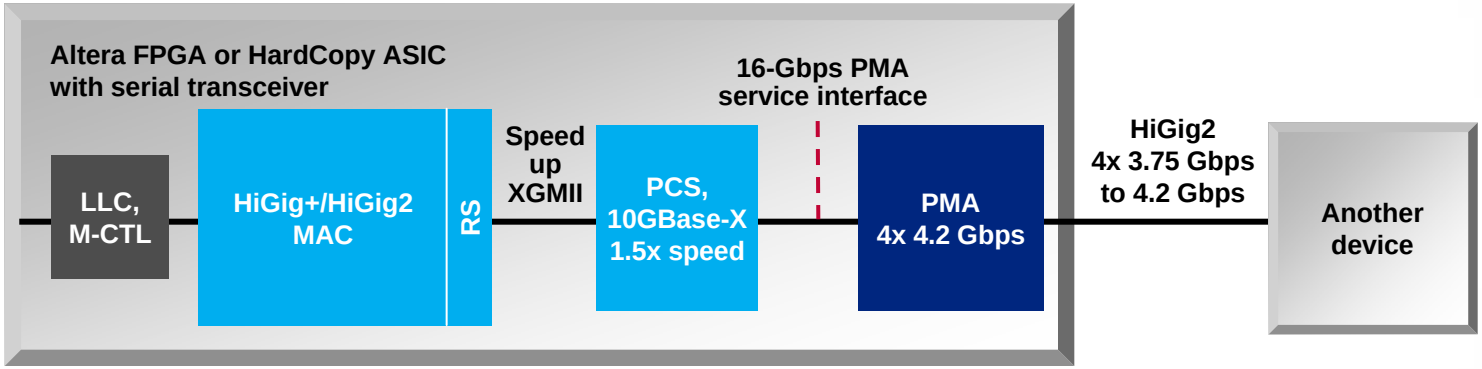


10 Gbps with RXAUI for chip to chip and chip to backplane

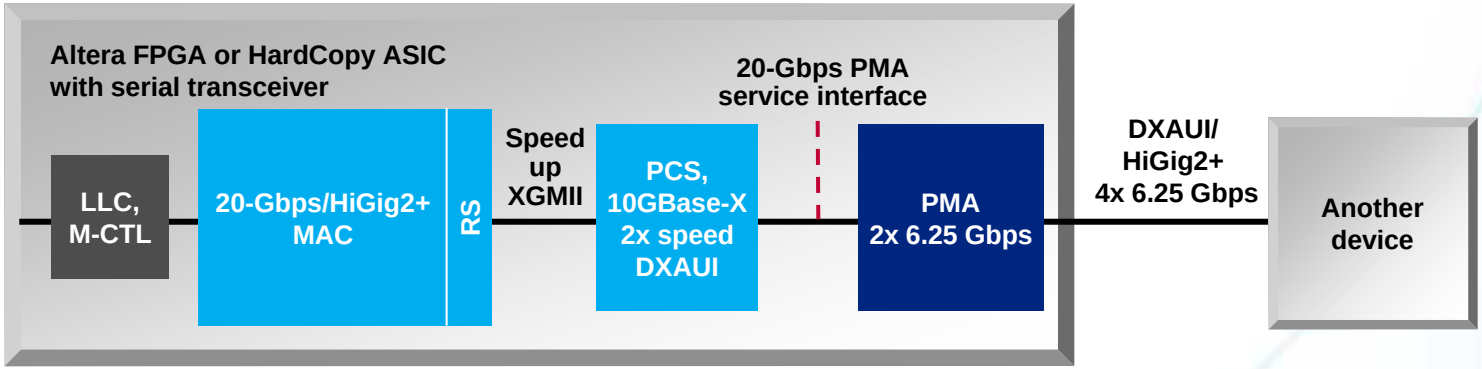
Soft IP **Hard IP**

Up to 20 GbE Blocks and Interfaces

4x 4.2-Gbps or 4x 6.25-Gbps Transceivers



15 Gbps with HiGig2 with 4-Gbps serial transceivers



20 Gbps with HiGig2+ or DXAUI for chip to chip and chip to backplane

Soft IP **Hard IP**