Designer Series Development System R1-1999 Release Notes

This document describes the new features and enhancements of the Designer Series Development System R1-1999 release. It also contains information about discontinued features and known limitations.

For information about which versions of Cadence, Mentor Graphics, Motive, Synopsys, and Viewlogic tools, and which versions of VHDL, and Verilog simulators are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com) and type "third party" (without quotes) in the keyword box.

New Features and Enhancements

This section lists the new features and enhancements of the R1-1999 release.

Devices and Packages

The R1-1999 release supports the following new devices and packages:

54SXA

54SXA is the new 0.25u 54SX family, which is supported in the following devices and packages:

A54SX32A – A new device, it is available for design in 208 PQFP, and 329 BGA packages.

54SX

54SX08 – An 84 PLCC package has been added.

ACT1

RT1020 – A new radiation tolerant device has been added and is available in the 84 CQFP package.

Designer

The Designer Series Development system now has the capability to perform timing-driven place and route for SX designs.

- Constraints for the place and route algorithms may be specified either with DT Edit, or by importing a Design Constraint File (.dcf file). Please see "*Designing With Actel*" for instructions on using DT Edit and DT Layout.

The SXA family of devices is supported in R1-1999 release. In order to design with this family, you must select 54SX as the family in the design setup window, and in the device selection window, you must select SXA from the new pull-down box.

Designer no longer will allow users to assign a signal to the TRST pin of RadTolerant devices. Please refer to the Radiation Tolerant device datasheet for details on the TRST pin.

ACTmap

The ACTgen macro inferring capabilities of ACTmap VHDL synthesis have been enhanced for the R1-1999 release.

- Accumulators, comparators, and XOR trees can now be inferred.

Please see the "*ACTmap VHDL Synthesis Methodology Guide*" for details.

- In ACTmap VHDL Compiler, the default optimization method has been changed from "Area" to "Speed".

The Default directory is no longer used as the working directory during VHDL synthesis. Whenever a VHDL design is compiled, a temporary directory called am##.tmp is created. All temporary files associated with synthesis are placed in this directory. The directory is then deleted once synthesis is complete.

ACTmap does not map to the DFPC(A) macro unless a preset/clear flip flop is explicitly inferred in the VHDL code. Since the DFPC(A) macro is implemented using two combinatorial cells, it is more efficient to map to sequential cell registers such as DFC1B.

BDD synthesis has been added to 54SX, and as a result, designs will compile more efficiently. Algorithms have also been modified to decrease run time on all families.

A block compile option has been introduced, which allows users to synthesize just a block of the design.

Silicon Expert

Silicon Expert is a production release in R1-1999. There are several significant changes from the previous Beta version that should be noted.

- Macro Manager wizard has been removed, so the I/O Macro manager and the Buffer Manager can only be invoked from the tools menu or the toolbar.
- All components of Silicon Expert have been enhanced with new interface features, better recognition of buffer trees and I/O macros, enhanced buffering, and overall efficiency improvements.

Please refer to the *Silicon Expert User's Guide* for details and instructions on using the tool.

Programming and Debugging

APSW has been modified to support the new "-1" Activator SX Adapter Modules. These Adapter Modules are required for programming .25µ SXA devices. Activator "-1" modules are backward compatible, and the previously released Activator SX Adapter Modules will continue to be supported for .35µ SX devices.

APSW has enhanced programming support for all devices. Enhancements include increased programming yield, and decreased programming times.

Actel is now shipping the Adaptec 1505A card, as opposed to the previously shipped 1505 card. Please consult the "Activator and APS Programming System User's Guide" for details of the installation process.

Silicon Sculptor

The Silicon Sculptor software version 2.01 is now available from the Designer install CD (Windows 95 and Windows 98 only).

To install the and invoke the software:

1. **Copy the "act_soft.exe" file from the "Sculptor" directory on the CD to your hard drive,**
2. **Double click "act_soft.exe."**
3. **To invoke the software: Double click the "Sculpt.exe" file on your hard drive.**

Make sure to check the Software Updates section in the User Area of our web site frequently for programming updates.

Silicon Explorer

None.

Cadence

SXA libraries have been added only to Concept. Composer user's who wish to use SXA devices should target their designs to SX and then follow the instructions in the "Known Limitations" Section for Designer.

Mentor Graphics

SXA libraries have been added.

MOTIVE

None.

Synopsys

Support for -F speed grade in the 40MX family, and –3 speed grade has been added to all MX devices in the R1-1999 release of Designer.

The SXA family has been added to the Synopsys libraries.

Viewlogic

SXA libraries have been added.

Verilog

SXA libraries have been added.

VHDL

SXA libraries have been added.

Macros

None.

Documentation

None

Discontinued Support

This section lists features that were supported in earlier versions of the Designer Series software, but are not supported in R1-1999 release.

Operating Systems

SunOS and HP9.X are no longer supported operating systems with the R1-1999 release of the Designer Series Development System.

Devices and Packages

54SX16P 329 BGA, and 272 BGA packages have been removed.

54SX32 272 BGA package has been removed.

ACTmap

The following options have been removed from ACTmap VHDL Synthesis:

Set Entity/Architecture

Max CPU time

ACTgen Macro Black Box

Sequential remapping (This is still available in netlist translate)

The following options have been removed from the Netlist Optimizer:

Max CPU time

Programming and Debugging

The R1-1999 version of APSW is not provided on the HP platform due to incompatibilities with all current versions of the HP-UX operating system. The last supported version of APSW on HP-UX is R3-1998, which runs only on HP 9.X.

Call the Actel Customer Applications Center for alternative programming options.

Known Limitations

This section lists the known limitations for the R1-1999 release. For the latest information on known limitations, check the GURU on-line technical support system on the Actel Web site (http://www.actel.com).

Devices and Packages

None.

Designer

Not all third party CAE tool support SXA devices. If the front-end tool you are using does not yet support the SXA family, you should use the libraries for SX in your design.

- In order to use the SXA family with a netlist targeted for the SX family, simply import the EDIF into Designer as you normally would, and instead of selecting SX in the device selection window, select SXA. If you plan to perform any type of structural simulation for an SXA design, it is required to export the structural VHDL or Verilog netlist from Designer.
- In order to convert a design from the SX family to the SXA family, it is required to re-import and re-compile the design netlist in Designer. It is also required to generate a new structural VHDL or Verilog netlist from Designer for simulation purposes.

DirectTime layout for SX designs does not fully support timing constraints on paths that include latches. If a constrained path passes through a latch, layout will fail, stating there are asynchronous loops in the design. Layout will also fail if a constraint is set on a path that starts or ends with a latch, stating there are non-applicable constraints.

and it will say there are non-applicable constraints if you set a constraint that either starts with or ends with a latch.

ACTmap

None.

ACTgen

None.

Silicon Expert

Networks that are directly driven by an I/O can not be viewed in Buffer Manager.

Silicon Explorer

To read the checksum of an ACT 1 or a 40MX device, you must connect the SDO connector from the Probe Pilot to the PRA pin of the FPGA.

In order to read the checksum from all devices, you must double click on the word “Checksum” in the Silicon Explorer software.

If you are having trouble probing a 3200DX device, please visit the Software Updates section of our web site in the User’s Area, and visit Guru, our automated on-line tech support system for updates to the Silicon Explorer software.

Silicon Explorer does not currently support SXA devices. SXA devices will be supported in a future release. Check Actel’s web site for updates of the Silicon Explorer software and with your local sales representative for availability.

Programming and Debugging

- The 54SX family does not support silicon signatures. If a silicon signature is used, a checksum error will result during programming.
- The Debugger tool in APSW does not support the 54SX device family.
- Designer does not support translation to Data I/O programming format (DIO) for the 54SX device family.
- APSW does not run on HP-UX 10.X. Call the Actel Customer Applications Center at 1-800-262-1060 for alternative programming options.
- APSW does not support SXA devices.

Silicon Sculptor

No programming support for SXA.

Cadence

Actel only supports the Concept-SCALD flow when using version PE 13.0.

Mentor Graphics

None.

MOTIVE

None.

Synopsys

None.

Viewlogic

Intelliflow or mixed schematic/HDL designs are not supported. Support is available from Viewlogic for direct Viewlogic customers.

Verilog

None.

VHDL None.

Macros None.

Documentation None.