Viewlogic® Powerview

Interface Guide

Actel

UNIX® Environments

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Introduction

The *Viewlogic Powerview Interface Guide* contains information about using the Viewlogic Powerview CAE software tools with the Actel Designer Series FPGA development software tools to create designs for Actel devices. Refer to the *Designing with Actel* manual for additional information about using the Designer series software and the Viewlogic documentation for additional information about using the Powerview software.

Document Organization

The *Viewlogic Powerview Interface Guide* is divided into the following chapters:

Chapter 1 - Setup contains information and procedures about setting up the Powerview software for use in creating Actel designs.

Chapter 2 - Design Flow illustrates and describes the design flow for creating Actel designs using the Powerview and Designer Series software.

Chapter 3 - Actel-Viewlogic Design Considerations contains information and procedures to assist you in creating Actel designs with the Powerview and Designer Series software.

Chapter 4 - Simulation Using ViewSim® contains information and procedures about simulating Actel designs with ViewSim.

Chapter 5 - Simulation Using SpeedWave™ contains information and procedures about simulating Actel designs with SpeedWave.

Appendix A - Product Support provides information about contacting Actel for customer and technical support.

Document Assumptions

The information in this guide is based on the following assumptions:

1. You have installed the Designer Series software.
2. You have installed the Powerview software.

3. You are familiar with UNIX workstations and operating systems.
4. You are familiar with FPGA architecture and FPGA design software.

Document Conventions

The following conventions are used throughout this manual.

Information that is meant to be input by the user is formatted as follows:

```
keyboard input
```

The contents of a file is formatted as follows:

```
file contents
```

Messages that are displayed on the screen appear as follows:

```
Screen Message
```

The <act_fam> variable represents an Actel device family. To reference an actual family, substitute the name of the Actel device when you see this variable. Available families are act1, act2 (for ACT 2 and 1200XL devices), act3, 3200dx, 40mx, 42mx, and 54sx.

The <vhd_fam> variable represents Compiled VHDL libraries. To reference an actual compiled library, substitute the name of the library (act1, act2 (for ACT 2 and 1200XL devices), act3, a3200dx, a40mx, a42mx, and a54sx) when you see this variable. Compiled VHDL libraries must begin with an alpha character.

Actel Manuals

The Designer Series software includes printed and on-line manuals. The on-line manuals are in PDF format on the CD-ROM in the "/manuals" directory. These manuals are also installed onto your system when you install the Designer software. To view the on-line manuals, you must install Adobe® Acrobat Reader® from the CD-ROM.

The Designer Series includes the following manuals, which provide additional information on designing Actel FPGAs:

Designing with Actel. This manual describes the design flow and user interface for the Actel Designer Series software, including information about using the ACTgen Macro Builder and ACTmap VHDL Synthesis software.

Actel HDL Coding Style Guide. This guide provides preferred coding styles for the Actel architecture and information about optimizing your HDL code for Actel devices.

ACTmap VHDL Synthesis Methodology Guide. This guide contains information, optimization techniques, and procedures to assist designers in the design of Actel devices using ACTmap VHDL.

Silicon Expert User's Guide. This guide contains information and procedures to assist designers in the use of Actel's Silicon Expert tool.

DeskTOP Interface Guide. This guide contains information about using the integrated VeriBest® and Synplicity® CAE software tools with the Actel Designer Series FPGA development tools to create designs for Actel Devices.

Cadence® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Cadence CAE software and the Designer Series software.

Mentor Graphics® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Mentor Graphics CAE software and the Designer Series software.

MOTIVE™ Static Timing Analysis Interface Guide. This guide contains information and procedures to assist designers in the use of the MOTIVE software to perform static timing analysis on Actel designs.

Synopsys® Synthesis Methodology Guide. This guide contains preferred HDL coding styles and information and procedures to assist designers in the design of Actel devices using Synopsys CAE software and the Designer Series software.

Viewlogic Powerview® Interface Guide. This guide contains information and procedures to assist designers in the design of Actel

devices using Powerview CAE software and the Designer Series software.

Viewlogic Workview Office Interface Guide. This guide contains information and procedures to assist designers in the design of Actel devices using Workview Office CAE software and the Designer Series software.

VHDL Vital Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Vital compliant VHDL simulator.

Verilog Simulation Guide. This guide contains information and procedures to assist designers in simulating Actel designs using a Verilog simulator.

Activator and APS Programming System Installation and User's Guide. This guide contains information about how to program and debug Actel devices, including information about using the Silicon Explorer diagnostic tool for system verification.

Silicon Sculptor User's Guide. This guide contains information about how to program Actel devices using the Silicon Sculptor software and device programmer.

Silicon Explorer Quick Start. This guide contains information about connecting the Silicon Explorer diagnostic tool and using it to perform system verification.

Designer Series Development System Conversion Guide UNIX® Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for UNIX to be compatible with later versions of Designer Series.

Designer Series Development System Conversion Guide Windows Environments. This guide describes how to convert designs created in Designer Series versions 3.0 and 3.1 for Windows to be compatible with later versions of Designer Series.

Actel FPGA Data Book. This guide contains detailed specifications on Actel device families. Information such as propagation delays, device package pinout, derating factors, and power calculations are found in this guide.

Macro Library Guide. This guide provides descriptions of Actel library elements for Actel device families. Symbols, truth tables, and module count are included for all macros.

A Guide to ACTgen Macros. This Guide provides descriptions of macros that can be generated using the Actel ACTgen Macro Builder software.

On-Line Help

The Designer Series software comes with on-line help. On-line help specific to each software tool is available in Designer, ACTgen, ACTmap, Silicon Expert, Silicon Explorer, Silicon Sculptor, and APSW.

1 Setup

This chapter contains information about setting up the Powerview software to create designs for Actel devices. Refer to the Viewlogic documentation for additional information about setting up Powerview.

Software Requirements

The information in this guide applies to the Actel Designer Series software release R2-1998 or later and Viewlogic Powerview. For specific information about which versions are supported with this release, go to the Guru automated technical support system on the Actel Web site (http://www.actel.com/guru) and type the following in the Keyword box:

```
third party
```

System Setup

After installing Powerview, make sure the proper environment variables are set in your UNIX shell script. The following are C shell variables. If you are using another shell, adjust the syntax accordingly.

```
setenv ALSDIR <actel_install_directory>
setenv WDIR <powerview_install_directory>
set path=($ALSDIR/bin $path)
```

If you use SunOS or Solaris, the following variable must also be set:

```
setenv LD_LIBRARY_PATH $ALSDIR/lib
```

If you use HP-UX, the following variable must also be set:

```
setenv SHLIB_PATH $ALSDIR/lib
```

If you use SpeedWave, the following variable must also be set:

```
setenv VANTAGE_VSS <vantage_install_directory>
```

Refer to the *Designing with Actel* manual and the Viewlogic documentation for additional information about setting environment variables.

Actel Libraries

The Actel libraries contain models for each Actel macro in all Actel families for use in Viewlogic. The Actel libraries are sufficient for most cases. Refer to “Migration Libraries” on page 2 for exceptions to using the Actel libraries.

The Powerview software uses a “viewdraw.ini” file to access the Actel libraries. Actel has provided template “viewdraw.ini” files in the “$ALSDIR/lib/wv/<act_fam>” directories that you can use. If you manually add the paths, they must be the first paths specified in the directories section of your “viewdraw.ini” file.

To access the Actel libraries:

Add the following lines to your “viewdraw.ini” file:

```
dir [p] .
dir [rm] $ALSDIR/lib/wv/<act_fam>/cells (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/actgen (ACTGEN)
dir [rm] $ALSDIR/lib/wv/sim (ACTELSIM)
dir [rm] $WDIR/lib/builtin (builtin)
```

For example, to configure Powerview to use the ACT 3 family library, replace “<act_fam>” with “act3” in the lines above.

Migration Libraries

In addition to the Actel libraries, Actel provides a set of migration libraries. These libraries contain macros that were supported in earlier versions of the Designer Series software and macros that may be needed to retarget designs from a different Actel family. If you are upgrading from a previous version of Designer and you have existing Actel designs, you must use the migration libraries. Actel does not recommend using the migration libraries on new designs.

The Powerview software uses a “viewdraw.ini” file to access the Actel libraries. Actel has provided template “viewdraw.ini” files in the “$ALSDIR/lib/wv/<act_fam>” directories that you can use. If you manually add the paths, they must be the first paths specified in the directories section of your “viewdraw.ini” file.

To access the migration libraries:

Add the following lines to your "viewdraw.ini" file:

```
dir [p] .
dir [rm] $ALSDIR/lib/wv/<act_fam>/cells (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELCELLS)
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELMIGRATE)
dir [rm] $ALSDIR/lib/wv/<act_fam>/migrate (ACTELMODELS)
dir [rm] $ALSDIR/lib/wv/actgen (ACTGEN)
dir [rm] $ALSDIR/lib/wv/sim (ACTELSIM)
dir [rm] $WDIR/lib/builtin (builtin)
```

For example, to configure Powerview to use the ACT 3 family library, replace "<act_fam>" with "act3" in the lines above.

Compiling Actel VITAL Libraries

Before simulating VHDL netlists that reference Actel macros in SpeedWave, you must compile Actel VITAL libraries. Use the following procedure to compile an Actel VITAL library.

1. **Create a directory called "swave" in the "/$ALSDIR/lib/vtl/95" directory.**
2. **Change to the "/$ALSDIR/lib/vtl/95/swave" directory.**
3. **Create and map the library directory for your simulator.** Compiled VITAL library names must begin with an alpha character. Type the following command at the prompt:

   ```
   vanlibcreate $ALSDIR/lib/vtl/95/swave/<vhd_fam> <vhd_fam>
   ```

   For example, to create and map the 40MX library for your simulator, type the following command:

   ```
   vanlibcreate $ALSDIR/lib/vtl/95/swave/a40mx a40mx
   ```

4. **Compile the library.** Compiled VITAL library names must begin with an alpha character. Type the following command at the prompt:

   ```
   analyze -src ../<act_fam>.vhd -lib <vhd_fam> -libieee -lib
   $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

   For example, to compile the 40MX library, type the following command:

   ```
   analyze -src ../40mx.vhd -lib a40mx -libieee -lib
   $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

5. **(Optional) Compile the migration library.** If your are using the migration library, type the following command at the prompt:

   ```
   analyze -src ../<act_fam>_mig.vhd -lib <vhd_fam> -libieee
   -lib $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

   For example, to compile the 40MX migration library, type the following command:

   ```
   analyze -src ../40mx_mig.vhd -lib a40mx -libieee -lib
   $VANTAGE_VSS/pgm/lib/synopsys.lib
   ```

Project Setup

You must set up an Actel project in the Viewlogic Project Manager for each Actel design before creating your design in Viewlogic. Use the following procedure to set up an Actel project in Powerview.

1. **Invoke Powerview.**
2. **Create a project.** Choose the Create command from the Project menu. The Create Project window is displayed.
3. **Set the Primary Directory.** Type the full path name of your design directory or use the Browse button. A “viewdraw.ini” file and the “pkt,” “sch,” “sym,” and “wir” directories are created.

4. **Configure the "viewdraw.ini" file.** Add the appropriate paths at the end of the "viewdraw.ini" file as shown in "Actel Libraries" on page 2. You can also copy one of the template "viewdraw.ini" files provided in the "/$ALSDIR/lib/wv/<act_fam>" directory of the Actel family you are targeting and modify the library paths listed in the last four lines, each beginning with a DIR.
5. **Verify your Current Project and Current Library paths.** From the Powerview Cockpit, make sure that the Current Project and Current Library under the Tool Status point to the primary directory.

2

Actel-Viewlogic Design Flow

This chapter illustrates and describes the design flow for creating Actel designs using the Powerview and Designer Series software.

Schematic-Based Design Flow Illustrated

Figure 2-1 shows the schematic-based design flow for creating an Actel device using the Powerview and Designer Series software[1].

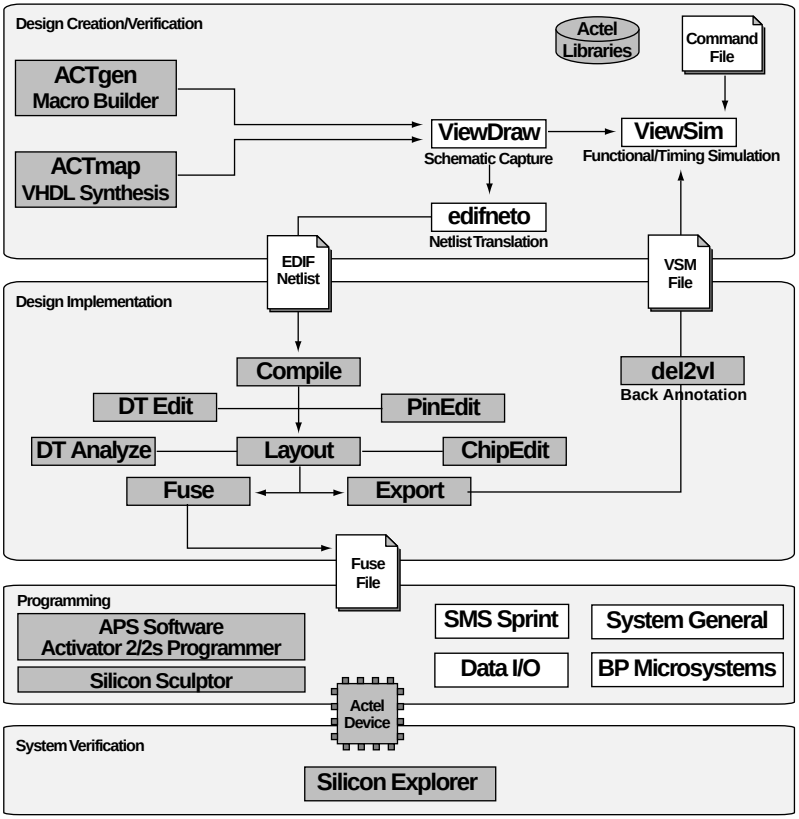

Figure 2-1. Actel-Viewlogic Schematic-Based Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-1.

Schematic-Based Design Flow Overview

The Actel-Viewlogic schematic-based design flow has four main steps; design creation/verification, design implementation, programming, and system verification. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, a schematic representation of a design is captured using the Viewlogic ViewDraw software. After design capture, a pre-layout (functional) simulation can be performed with the Viewlogic ViewSim software. Finally, an EDIF netlist is generated for use in Designer.

Schematic Capture

Enter your schematic in ViewDraw. Refer to chapter 3, "Actel-Viewlogic Design Considerations" on page 15 and the Viewlogic documentation for information about using ViewDraw.

Functional Simulation

Perform a functional simulation of your design using ViewSim before generating an EDIF netlist for place and route. Functional simulation verifies that the logic of the design is correct. Unit delays are used for all gates during functional simulation. Refer to "Functional Simulation" on page 21 and the Viewlogic documentation for information about performing functional simulation.

EDIF Netlist Generation

After you have captured and verified your design, you must generate an EDIF netlist for place and route in Designer. Refer to "Generating an EDIF Netlist" on page 19 for information about generating an EDIF netlist.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis can be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with the Viewlogic ViewSim software.

Place and Route

Use Designer to place and route your design. Make sure you specify VIEWLOGIC as the Edif Flavor and Generic as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designing with Actel* manual for information about using Designer.

Static Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis on your design. Refer to the *Designing with Actel* manual for information about using DT Analyze.

Timing Simulation

Perform a timing simulation of your design using ViewSim after placing and routing it in Designer. Timing simulation requires information extracted and back annotated from Designer. Refer to "Timing Simulation" on page 21 and the Viewlogic documentation for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing with Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

VHDL Synthesis-Based Design Flow Illustrated

Figure 2-2 shows the VHDL synthesis-based design flow for an Actel device using the Powerview and Designer Series software[1].

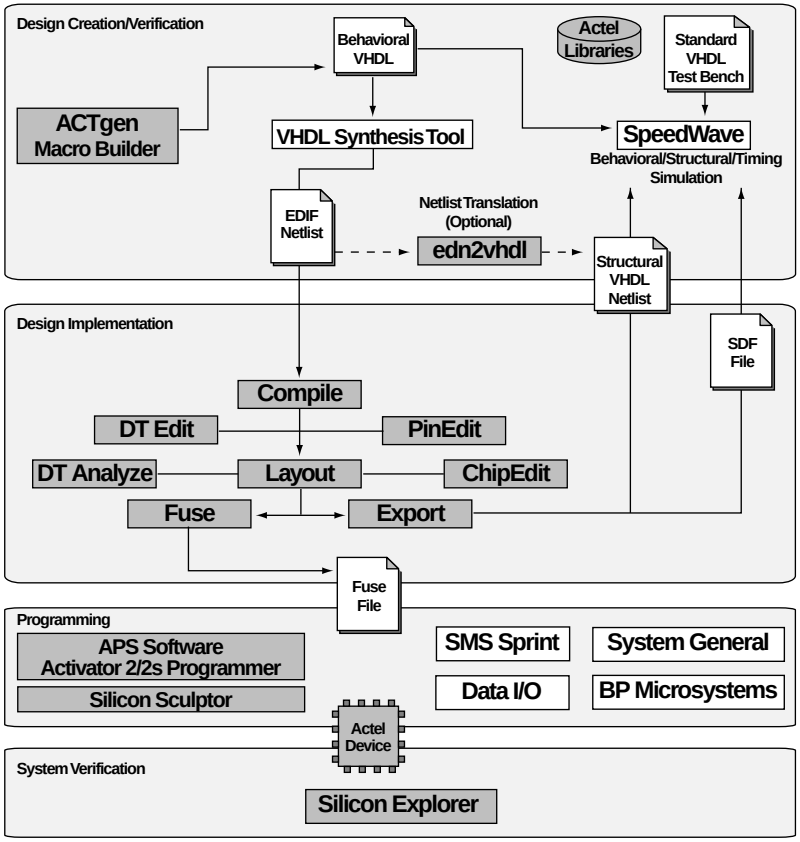

Figure 2-2. Actel-Viewlogic VHDL Synthesis-Based Design Flow

1. Actel-specific utilities/tools are denoted by the grey boxes in Figure 2-2.

VHDL Synthesis-Based Design Flow Overview

The Actel-Viewlogic VHDL synthesis-based design flow has four main steps; design creation/verification, design implementation, programming, and system verification. These steps are described in the following sections.

Design Creation/ Verification

During design creation/verification, a design is captured in an RTL-level (behavioral) VHDL source file. After capturing the design, a behavioral simulation of the VHDL file can be performed with the Viewlogic SpeedWave software to verify that the VHDL code is correct. The code is then synthesized into a structural VHDL netlist. After synthesis, a structural simulation of the design can be performed. Finally, an EDIF netlist is generated for use in Designer and a VHDL structural netlist is generated for structural and timing simulation in SpeedWave.

VHDL Design Source Entry

Enter your design source using a text editor or a context-sensitive VHDL editor. Your VHDL design source can contain RTL-level constructs as well as instantiations of structural elements, such as ACTgen macros.

Behavioral Simulation

Perform a behavioral simulation of your design before synthesis. Behavioral simulation verifies the functionality of your VHDL code. Typically, unit delays are used and a standard VHDL test bench can be used to drive simulation. Refer to “Behavioral Simulation” on page 25 and the Viewlogic documentation for information about performing behavioral simulation.

Synthesis

After you have created your behavioral VHDL source file, you must synthesize it before placing and routing it in Designer. Synthesis transforms the behavioral VHDL file into a gate-level netlist and optimizes the design for a target technology. Refer to the documentation included with your synthesis tool for information about performing design synthesis.

EDIF Netlist Generation

After you have created, synthesized, and verified your design, you must generate an EDIF netlist for place and route in Designer. This EDIF netlist is also used to generate a structural VHDL netlist. Refer to "Generating an EDIF Netlist" on page 19 for information about generating an EDIF Netlist.

Structural VHDL Netlist Generation

Generate a structural VHDL netlist from your EDIF netlist for use in structural and timing simulation by either exporting it from Designer or by using the Actel "edn2vhdl" program. Refer to "Generating a Structural VHDL Netlist" on page 19 for information about generating a structural VHDL netlist.

Structural Simulation

Perform a structural simulation of your design before placing and routing it. Structural simulation verifies the functionality of your post-synthesis structural VHDL netlist. Unit delays included in the compiled Actel VHDL libraries are used for every gate. Refer to "Structural Simulation" on page 26 and the Viewlogic documentation for information about performing structural simulation.

Design Implementation

During design implementation, a design is placed and routed using Designer. Additionally, static timing analysis can be performed on a design in Designer with the DT Analyze tool. After place and route, post-layout (timing) simulation is performed with the Viewlogic SpeedWave software.

Place and Route

Use Designer to place and route your design. Make sure to specify GENERIC (or VIEWLOGIC if you are using a Viewlogic synthesis tool) as the Edif Flavor and VHDL as the Naming Style when importing the EDIF netlist into Designer. Refer to the *Designing with Actel* manual for information about using Designer.

Static Timing Analysis

Use the DT Analyze tool in Designer to perform static timing analysis of your design. Refer to the *Designing with Actel* manual for information about using DT Analyze.

Timing Simulation

Perform a timing simulation of your design after placing and routing it. Timing simulation requires information extracted from Designer, which overrides unit delays in the compiled Actel VHDL libraries. Refer to "Timing Simulation" on page 27 and the Viewlogic documentation for information about performing timing simulation.

Programming

Program a device with programming software and hardware from Actel or a supported 3rd party programming system. Refer to the *Designing with Actel* manual and the *Activator and APS Programming System Installation and User's Guide* or *Silicon Sculptor User's Guide* for information about programming an Actel device.

System Verification

You can perform system verification on a programmed device using the Actel Silicon Explorer diagnostic tool. Refer to the *Activator and APS Programming System Installation and User's Guide* or *Silicon Explorer Quick Start* for information about using the Silicon Explorer.

3

Actel-Viewlogic Design Considerations

This chapter contains information and procedures to assist you in creating Actel designs with Viewlogic Powerview software. This includes schematic design considerations and netlist generation procedures.

Schematic Naming Conventions

Use only alphanumeric and underscore "_" character for schematic net and instance names. Do not use asterisks, forward and backward slashes, spaces, or periods.

Adding Power and Ground

To add power or ground signals in the schematic, use the Actel VCC or GND symbols. You can also label the nets as VDD or GND.

Adding Pins to the Design

Add pins to the top-level schematic of the design by using the I/O buffer macros with a dangling net attached to the pad, as shown in Figure 3-1. The label on the dangling net becomes the I/O pin name.

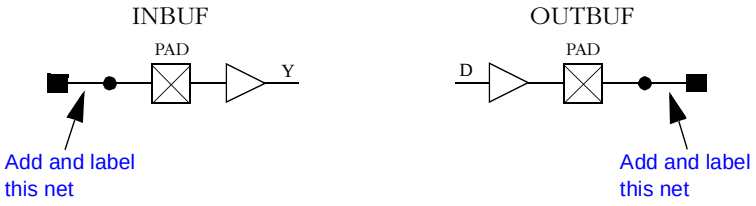

Figure 3-1. Adding Pins to a design

Generating a Top-Level Symbol

When generating a top-level symbol, ViewGen looks for an In or Out port. The convention is illustrated in Figure 3-2. ViewGen does not generate symbols for schematics without IN/OUT ports. The IN/OUT ports are found in the "$ALSDIR/lib/wv/asicbin" directory.

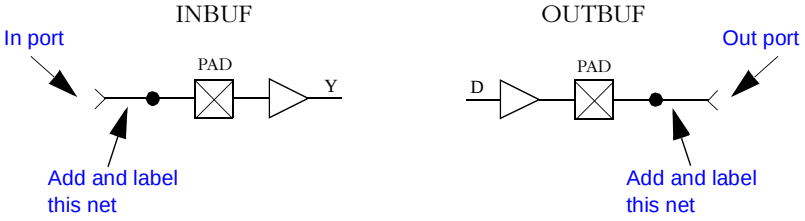

Figure 3-2. Input/Output Ports

Buried I/O

I/O macros can be buried in the design hierarchy.

Sheets and Symbols

A multiple-page design is composed of more than one schematic file or <design>.n file in the schematic directory. For a multiple-page design, each sheet is treated as a part of a top-level schematic and is not considered a hierarchy level.

Assigning Pins in a Schematic

Nets in your schematic that have the "PIN" attribute assigned to them in ViewDraw are automatically assigned to that pin during design implementation in Designer.

To assign the "PIN" attribute to a net in ViewDraw:

1. **Select the net to assign pin information.**
2. **Add a Pin attribute to the net.** Select the Attr command from the Add menu. The Add Attribute dialog box is displayed. Type the following in the Attribute box:

   ```
   pin=<valid_pin_number>
   ```

   Click OK.

Note: This procedure assigns the pin name to the signal net in the netlist. If you use this method to fix pins, and you change your pin assignments in PinEdit, you will not be able to back annotate. PinEdit does not change netlist information.

Adding ACTgen Macros

The ACTgen Macro Builder can automatically generate symbols that can be added to your schematic. The following steps describe the procedure.

1. **Invoke ACTgen.**
2. **Select the family, macro type, and macro options.**
3. **Generate your macro as a Viewlogic symbol.** Make sure that you specify Viewlogic as the Netlist/CAE Formats in the Generate Macro dialog box.
4. **Add the macro as a component in the schematic.** Refer to the Viewlogic documentation for information about adding components to a schematic.

Refer to the *Designing With Actel* manual or the ACTgen on-line help for additional information about using ACTgen.

Adding ACTmap Blocks

The ACTmap VHDL Synthesis tool can generate symbols from VHDL blocks that can be added to your schematic. The following steps describe the procedure.

1. **Invoke ACTmap.**
2. **Open the ACTmap VHDL Compiler window.** Select the VHDL Compiler command from the File menu.
3. **Compile your VHDL block and generate an EDIF netlist.** Type the name of your design in the Source Design box or use the Browse button. Specify Block as the Mode, select options, and click the Run button. The Main window displays a report of the compilation process.
4. **Translate the EDIF netlist to a Viewlogic symbol.** Click the Translate button in the ACTmap VHDL Compile window. Type the name of your VHDL block in the Source Design box or use the Browse button. Specify Viewlogic as the Output Format, select options, and click the Run button.
5. **Set VL options.** In the Set VL dialog box, make sure the symbol check box is marked. The other check boxes are optional. Click OK.
6. **Add the block as a component in the schematic.** Refer to the Viewlogic documentation for information about adding components to a schematic.

   Note: ACTmap supports hierarchical EDIF output, but the symbol generator only creates the top level symbol.

Refer to the *Designing with Actel* manual, the *ACTmap VHDL Synthesis Methodology Guide*, or the ACTmap on-line help for additional information about using ACTmap.

Generating an EDIF Netlist

The EDIF netlist is used for place and route in Designer. To generate an EDIF netlist from Powerview, choose the following options in the Powerview “edifneto” window:

Select type:	Hierarchical netlist
Wire file name:	<design_name>
Level:	Hard
Output filename:	<design_name>.edn
Port/Supply type config file:	ediftype.cfg

To generate an EDIF netlist from a synthesis-based design:

Refer to the documentation included with your synthesis tool for information about generating an EDIF netlist.

Generating a Structural VHDL Netlist

You can generate a structural VHDL netlist from your EDIF netlist by either exporting it from Designer or by using the “edn2vhdl” program. The structural VHDL netlist generated by Designer and the “edn2vhdl” use std_logic for all ports. The bus ports are in the same bit order as they appear in the EDIF netlist.

Note: If you are using ACTmap, use it to generate the structural VHDL netlist.

To generate a structural VHDL netlist using Designer:

1. **Invoke Designer.**
2. **Import your EDIF netlist.** Select the Import Netlist command from the File menu. The Import Netlist dialog box is displayed. Specify EDIF as the Netlist Type, GENERIC (or VIEWLOGIC if you are using a Viewlogic synthesis tool) as the Edif Flavor, and VHDL as the Naming Style. Type the full path name of your EDIF netlist or use the Browse button to select your design. Click OK.

3. **Export a structural VHDL netlist.** Select the Export command from the File menu. The Export dialog box is displayed. Specify Netlist File as the File Type and VHDL as the Format. Click OK.

To generate a structural VHDL netlist using edn2vhdl:

1. **Change to the directory that contains the EDIF netlist.**
2. **Type the following command at the prompt:**

```
edn2vhdl fam:<act_fam> <design_name>
```

4

Simulation Using ViewSim

This chapter describes the procedures for performing functional and timing simulations of your Actel design using the Viewlogic ViewSim simulation tool.

Functional Simulation

Use the following procedure to perform a functional simulation of an Actel design:

1. **Select your Actel project in the Powerview Cockpit.** If you have not created or setup your project, go to "Project Setup" on page 4 for the procedure.
2. **Open the ViewSim Wirelister dialog box.** Invoke VSM from the Powerview Cockpit.
3. **Generate a simulation (.vsm) wirelist.** Type in the design name and click OK. A simulation wirelist is generated.
4. **Simulate the design.** Invoke ViewSim from the Powerview Cockpit. Type in the design name in the Design Name box and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

Timing Simulation

Use the following procedure to perform a timing simulation of an Actel design:

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a <design_name>.stf file by choosing the GENERIC option from the CAE pull-down menu. Click OK.

3. **Back annotate your delays.** Type the following command at the prompt:

   ```
   del2vl <design_name>
   ```

   The <design_name>.stf in the current directory is read and a <design_name>.dtb and <design_name>.vsm file is generated for use with ViewSim.

4. **Select your Actel project in the Powerview Cockpit.** If you have not created or setup your project see "Project Setup" on page 4.

5. **Simulate the design.** Invoke ViewSim from the Powerview Cockpit. Type in the design name in the Design Name box and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

Multichip Simulation

System designs are typically divided into functional modules that are implemented by several Actel devices. To check the functionality of the system, all Actel devices must be simulated together. You can use ViewSim and Designer to perform multichip simulation. Use the following procedure to perform a multichip simulation of an Actel design:

Note: Because the viewdraw.ini file uses the same alias for all Actel families, you can only simulate multiple Actel devices of the same family.

1. **Create a top level schematic and instantiate the individual chip designs.** This example, assumes there are three designs with instance names "chip1," "chip2," and "chip3." The name of the top level schematic is "top." Figure 4-1 depicts the directory structure

for this example. Names written in normal text represent file names and those in bold text represent directory names.

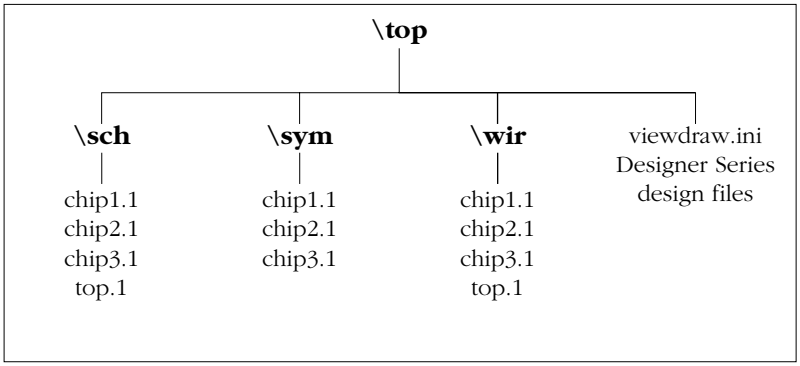

Figure 4-1. Directory Structure for Multichip Simulation

Note: This example only contains single-sheet schematics for each design. Similar procedures apply to multiple-sheet designs.

2. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
3. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a "chip1.stf" file by choosing the GENERIC option from the CAE pull-down menu. Click OK. Repeat for "chip2.stf" and "chip3.stf."
4. **Back annotate your delays.** Make sure you are in the "\top" directory and Type the following command at the prompt:

   ```
   del2vl chip1
   ```

   The "chip1.stf" file is read and a "chip1.dtb" and "chip1.vsm" file is generated. Repeat for the "chip2.stf" and "chip3.stf" files.

5. **Create a "top.dtb" file for the top level schematic.** The top level DTB file should include the following lines:

```
.ba
c chip1
a dtb=chip1.dtb
c chip2
a dtb=chip2.dtb
c chip3
a dtb=chip3.dtb
.ab
```

   The "c" lines above specifies instance names, such as "chip1." If you haven't labeled an instance, you can use the default handle name of an instance, "$1I38" as it appears in your top-level schematic. Also, the individual DTB files should reside in the top level design directory, "top."

6. **Run ViewVSM on "top.dtb."** Reference the "top.dtb" file in the VSM pop-up dialog box. The VSM program processes the DTB files for each chip and creates the "top.vsm" file with back annotated post-layout timing delays.

7. **Simulate "top.vsm."** Invoke ViewSim from the Powerview Cockpit. Type "top.vsm" in the Design Name box and click OK.

Refer to the Viewlogic documentation for additional information about performing simulation with ViewSim.

5 Simulation Using SpeedWave

This chapter describes the procedures for performing simulations on an Actel design using the Viewlogic SpeedWave simulation tool.

Behavioral Simulation

Use the following procedure to perform a behavioral simulation of an Actel design:

Note: When installing the Viewlogic SpeedWave simulator, you have the option of installing a standard IEEE library or the Synopsys version.You must install the Synopsys libraries for compatibility with Actel VITAL libraries and you must include the Synopsys library in your invocations. The commands in this guide use the Synopsys version of the IEEE libraries.

1. **Create a working directory.** Type the following command at the prompt:

   ```
   vanlibcreate ./user.lib user
   ```

2. **Create a soft link to the synthesis library.** Type the following command at the prompt:

   ```
   ln -s $VANTAGE_VSS/pgm/libs/synopsys.lib synopsys
   ```

3. **Analyze your behavioral VHDL design files and test bench.** Type the following commands at the prompt:

   ```
   analyze -src <design_name>.vhd -lib user.lib -libieee -lib
   synopsys
   analyze -src <vhdl_test_bench>.vhd -lib user.lib -libieee
   -lib synopsys
   ```

4. **Map to the Actel VITAL and FPGA libraries.** If any Actel macros are instantiated in your VHDL source, you must add the following switches when analyzing your VHDL design files:

   ```
   analyze -src <design_name>.vhd -lib user.lib -lib $ALSDIR/
   lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
   ```

Add the following lines to your VHDL design files to reference the Actel Family library in your VHDL design files:

```
library <vhd_fam>;
use <vhd_fam>.components.all;
```

5. **Simulate your design.** Type the following command at the prompt:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys
```

If any Actel macros are instantiated in your VHDL source, you must simulate using the compiled Actel VHDL library for that family. For example, to simulate a configuration named "cfg_tb_behavior" for a 40MX device, type the following command at the prompt:

```
vbsim -cfg cfg_tb_behavior -until complete -lib user.lib
-libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

Structural Simulation

Use the following procedure to perform a structural simulation of an Actel design:

1. **Synthesize your design.** Refer to the documentation included with your synthesis tool for information about synthesis.
2. **Analyze the structural VHDL netlist and the test bench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 19 for the procedure. Type the following commands at the prompt to analyze the VHDL netlist and test bench:

```
analyze -src <design_name>.vhd -lib user.lib -lib $ALSDIR/
lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

```
analyze -src <vhdl_test_bench>.vhd -lib user.lib -lib $ALS-
DIR/lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

3. **Simulate your design.** Type the following command at the prompt:

```
vbsim -cfg <configuration_name> -until complete
-lib user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/
95/swave/<vhd_fam>
```

   For example, to simulate a configuration named "cfg_tb_structure" for a 40MX device, type the following command at the prompt:

```
vbsim -cfg cfg_tb_structure -until complete -lib user.lib -
libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/swave/a40mx
```

Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

Timing Simulation

Use the following procedure to perform a timing simulation of an Actel design:

1. **Place and route your design in Designer.** Refer to the *Designing with Actel* manual for information about using Designer.
2. **Extract timing information for your design.** Choose the Extract command from the Tools menu or click the Extract button. The Extract dialog box is displayed. Create a <design_name>.sdf file by specifying SDF as the CAE type. Click OK.
3. **Analyze the structural VHDL netlist and the test bench.** If you have not already generated a structural VHDL netlist, go to "Generating a Structural VHDL Netlist" on page 19 for the procedure. Type the following commands at the prompt to analyze the VHDL netlist and test bench:

```
analyze -src <design_name>.vhd -lib user.lib -lib $ALSDIR/
lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

```
analyze -src <vhdl_test_bench>.vhd -lib user.lib -lib
$ALSDIR/lib/vtl/95/swave/<vhd_fam> -libieee -lib synopsys
```

4. **Simulate your design.** Type the following command at the prompt:

```
vbsim -cfg <configuration_name> -until complete -lib
user.lib -libieee -lib synopsys -lib $ALSDIR/lib/vtl/95/
swave/<vhd_fam> -sdf <design_name>.sdf <UUT> -sdfmode
[min|typ|max]
```

   In the previous command, the <configuration_name> variable is the name of the configuration that binds the test bench entity and architecture, the <design_name> variable is the name of the top level entity, and the <UUT> variable is the instance of the top level entity in the test bench.

Refer to the Viewlogic documentation for additional information about performing simulation with SpeedWave.

A

Product Support

Actel backs its products with various support services including Customer Service, a Customer Applications Center, a Web and FTP site, electronic mail, and worldwide sales offices. This appendix contains information about using these services and contacting Actel for service and support.

Actel U.S. Toll-Free Line

Use the Actel toll-free line to contact Actel for sales information, technical support, requests for literature about Actel and Actel products, Customer Service, investor information, and using the Action Facts service.

The Actel Toll-Free Line is (888) 99-ACTEL.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call (408) 522-4480.
From Southeast and Southwest U.S.A., call (408) 522-4480.
From South Central U.S.A., call (408) 522-4434.
From Northwest U.S.A., call (408) 522-4434.
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From Europe, call (408) 522-4252 or +44 (0) 1256 305600.
From Japan, call (408) 522-4743.
From the rest of the world, call (408) 522-4743.
Fax, from anywhere in the world (408) 522-8044.

Customer Applications Center

The Customer Applications Center is staffed by applications engineers who can answer your hardware, software, and design questions.

All calls are answered by our Technical Message Center. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:30 a.m. to 5 p.m., Pacific Standard Time, Monday through Friday.

The Customer Applications Center number is (800) 262-1060.

European customers can call +44 (0) 1256 305600.

Guru Automated Technical Support

Guru is a Web based automated technical support system accessible through the Actel home page (**http://www.actel.com/guru/**). Guru provides answers to technical questions about Actel products. Many answers include diagrams, illustrations and links to other resources on the Actel Web site. Guru is available 24 hours a day, seven days a week.

Web Site

Actel has a World Wide Web home page where you can browse a variety of technical and non-technical information. Use a Net browser (Netscape recommended) to access Actel's home page.

The URL is **http://www.actel.com**. You are welcome to share the resources we have provided on the net.

Be sure to visit the "Actel User Area" on our Web site, which contains information regarding: products, technical services, current manuals, and release notes.

FTP Site

Actel has an anonymous FTP site located at **ftp://ftp.actel.com**. You can directly obtain library updates, software patches, design files, and data sheets.

Electronic Mail

You can communicate your technical questions to our e-mail address and receive answers back by e-mail, fax, or phone. Also, if you have design problems, you can e-mail your design files to receive assistance. The e-mail account is monitored several times per day.

The technical support e-mail address is **tech@actel.com**.

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