Using Silicon Explorer with SX FPGAs

Introduction

Actel's SX FPGAs have build in probe circuitry that is accessed and controlled by Silicon Explorer, an integrated verification and logic analysis tool that attaches to a PC's standard COM port. This application brief describes the internal probe circuitry contained in Actel's SX FPGAs that allows real-time observation and analysis of a device's internal logic nodes without design iteration. Silicon Explorer also functions as an 18-channel logic analyzer that samples data asynchronously at 100 MHz or synchronously at 66 MHz.

Silicon Explorer

Silicon Explorer integrates two verification tools, the Probe Instrument and the Timing Instrument, as shown in the Graphical User Interface (GUI) in Figure 1. The Probe Instrument lists all of the nets in the FPGA that can be observed. Two channels of the logic analyzer, which are directly connected to the PRA and PRB pins of an SX device, can automatically display any two signals inside the FPGA. By selecting the desired net in the list and then pressing the PRA or PRB button, the signal from that net is displayed on the Timing Instrument for analysis. The Timing Instrument is an 18-channel logic analyzer that automatically displays the signals of both the probe outputs and up to 16 additional signals on the target system. Silicon Explorer also has the ability to read-back the checksum of the design programmed into the device, enabling designers to verify that the correct design was programmed into the FPGA.

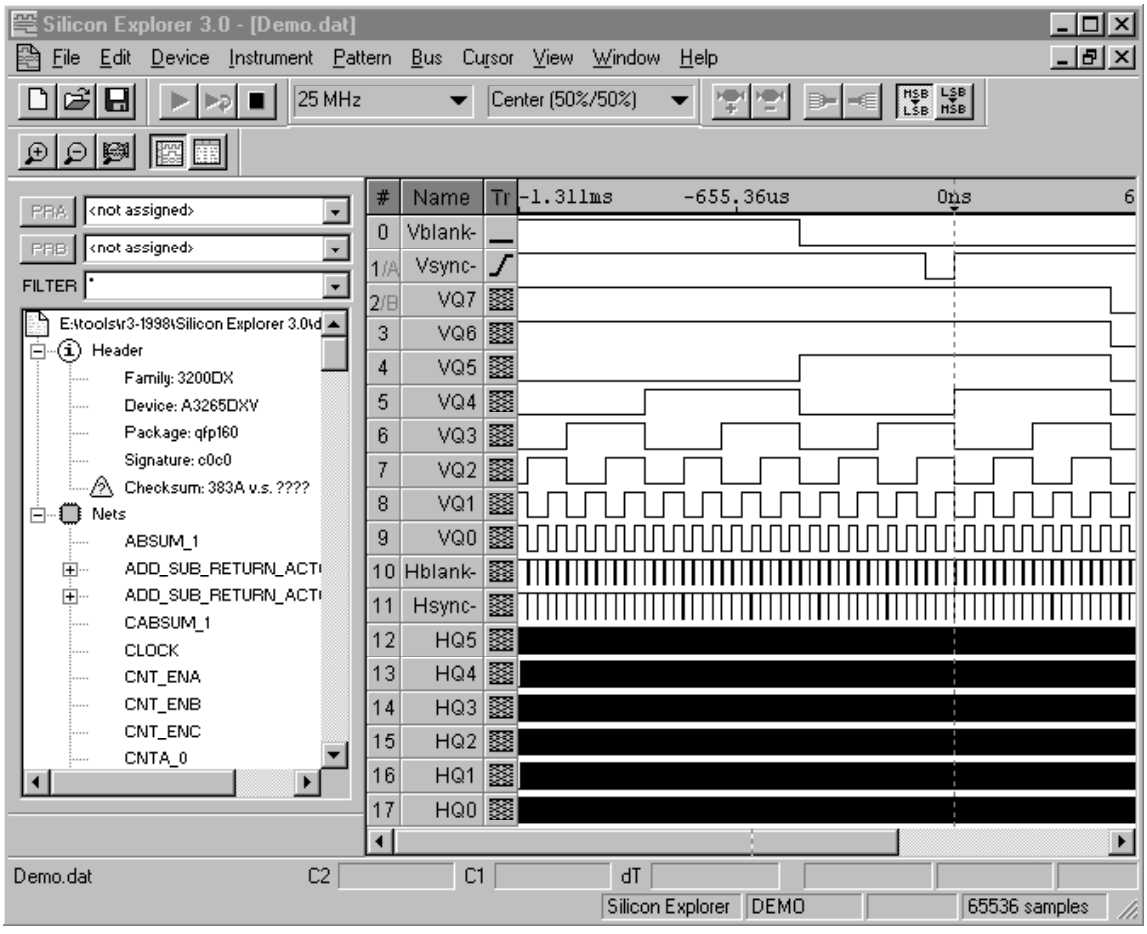

Figure 1 • *Silicon Explorer GUI*

SX Probe Circuit Control Pins

Silicon Explorer uses the JTAG ports (TDI, TCK, TMS, and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. Figure 2 illustrates the interconnection between Silicon Explorer and the FPGA to perform in-circuit verification. Figure 3 shows Silicon Explorer's pinouts. Note that SX devices do not have a Mode connector, so the Mode pin is not used in SX device verification. The JTAG TMS pin replaces the function provided by the Mode pin in other Actel devices.

Configuring Diagnostic Pins

The JTAG and Probe pins (TDI, TCK, TMS, TDO, PRA, and PRB) are placed in the desired mode by selecting the appropriate check boxes in the "Device Variations" dialog window, as shown in Figure 4. This dialog window is accessible through the Design Setup Wizard under the option menu in Actel's Designer software.

Dedicated JTAG mode

When the "Reserve JTAG Pin" box is checked, the FPGA is placed in Dedicated JTAG mode, which configures the TDI, TCK, and TDO pins for JTAG boundary scan or in-circuit verification with Silicon Explorer. An internal pull-up resistor is automatically enabled on both the TMS and TDI pins (see Figure 5). In addition, by checking the "Reserve JTAG Pin" box, TDI, TCK, and TDO are made unavailable for pin assignment in the Pin Editor.

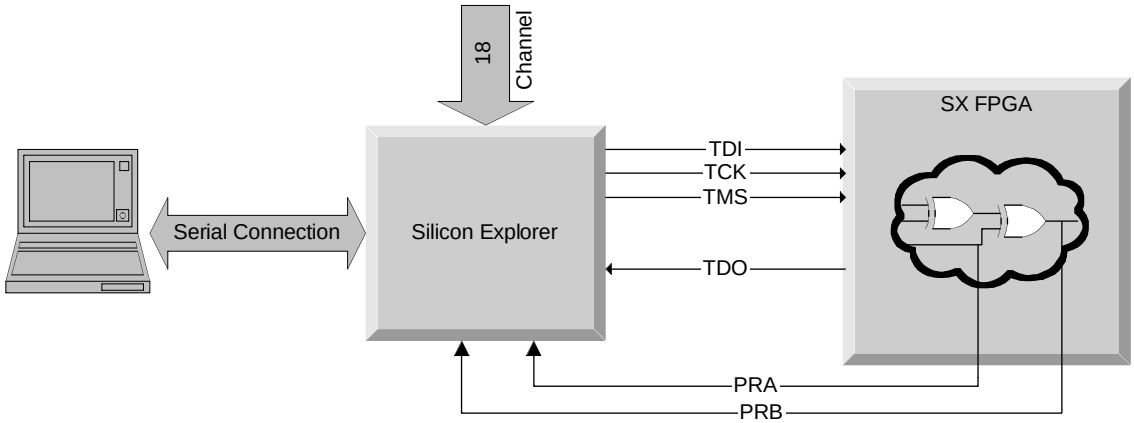

Figure 2 • *Probe Setup*

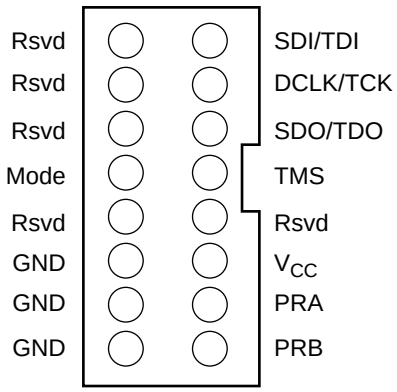

Figure 3 • *Silicon Explorer Pin-Out*

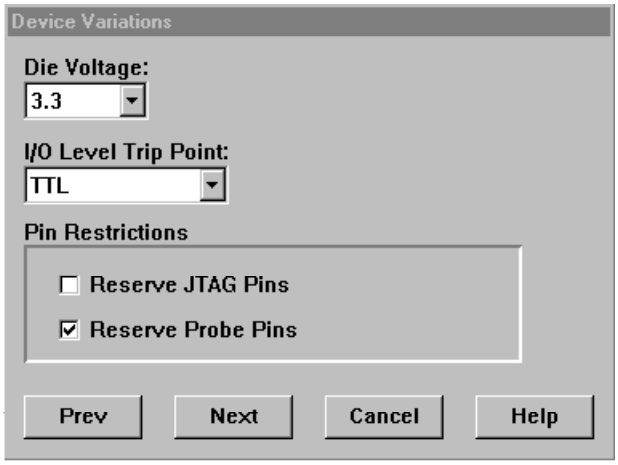

Figure 4 • *Diagnostic Pin Configuration*

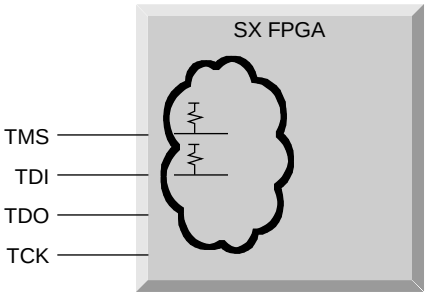

Figure 5 • *Dedicated JTAG Mode*

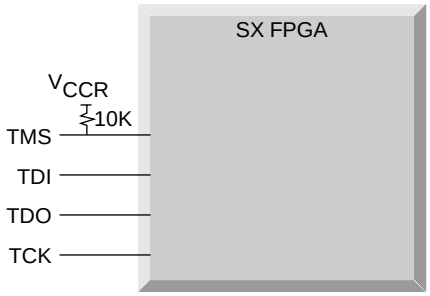

Figure 6 • *Flexible JTAG Mode*

Flexible JTAG mode

When the "Reserve JTAG Pin" box is not selected, the FPGA is placed in Flexible JTAG mode, which allows the TDI, TCK, and TDO pins to function as user I/Os or as JTAG pins. In this mode, the internal pull-up resistor on the TMS and TDI pins are disabled. An external 10KΩ pull-up resistor is required on the TMS pin (see Figure 6).

The TDI, TCK, and TDO pins are transformed from user I/Os into JTAG diagnostic pins when a rising edge at TCK is detected while TMS is at logical low. The JTAG pins revert to user I/Os when the JTAG state machine is placed in the Test-Logic reset state.

Table 1 shows the possible configurations of the diagnostic pins.

Reserving Probe Pins

When the "Reserve Probe Pin" box is selected, the layout tool is directed to reserve the PRA and PRB pins as diagnostic pins. This option is merely a guideline. If the Layout tool must use the PRA and PRB pins as user I/Os to achieve successful layout, these pins will not be reserved. If user I/Os are assigned to the PRA and PRB pins and the "Reserve Probe Pin" option is selected, the Layout tool will override the "Reserve Probe Pin" option.

Design Considerations

Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bi-directional ports. Since these pins are active during probing, critical input signal through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the Probe Circuit.

Conclusion

Actel's SX FPGAs include internal probe circuitry that allows 100% observability into a device's internal nodes. Silicon Explorer accesses this circuitry and provides an integrated set of features that enables quick and easy isolation of design problems without re-layout. With the real-time access into internal nodes offered by Silicon Explorer, designers can significantly accelerate the design verification process by removing the guesswork typically associated with trial-and-error methods of system verification.

Table 1 • *Diagnostic Pin Configuration*

Mode	Configuration
Dedicated JTAG Mode	TCK, TDI, and TDO are dedicated diagnostic pins.[1]
Flexible JTAG Mode	TCK, TDI, and TDO may be used as I/Os.[2]

Notes:

1. *No pull-up resistor required.*
2. *A 10KΩ pull-up resistor on the TMS Pin is required*

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