COEN 6501

Q1

Oct 2012

$N = n_3\, n_2\, n_1\, n_0$

$n_3\, n_2\, n_1\, n_0$

$n_3 n_0 \quad n_2 n_0 \quad n_1 n_0 \quad n_0 n_0$

$n_3 n_1 \quad n_2 n_1 \quad n_1 n_1 \quad n_1 n_0$

$n_3 n_2 \quad n_2 n_2 \quad n_1 n_2 \quad n_2 n_0$

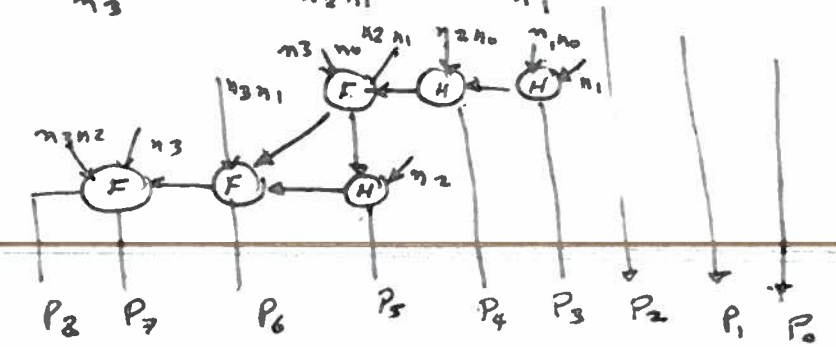
$n_3 n_3 \quad n_3 n_2 \quad n_3 n_1 \quad n_3 n_0$

$n_3 n_2 \quad n_3 n_1 \quad n_3 n_0 \quad n_2 n_0 \quad n_1 n_0 \quad 0 \quad n_0 \quad 0$ ↙ $2N^2$

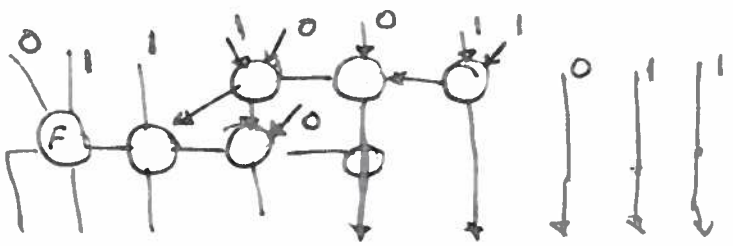
$n_3 \qquad n_2 n_1 \qquad n_1 \qquad 1 \quad +1$

$n_3 n_2 \quad n_3 n_1 \quad n_3 n_0 \quad n_2 n_0 \quad n_1 n_0 \quad 0 \quad n_0 \quad 1$

$n_3 \qquad n_2 n_1 \qquad n_1$



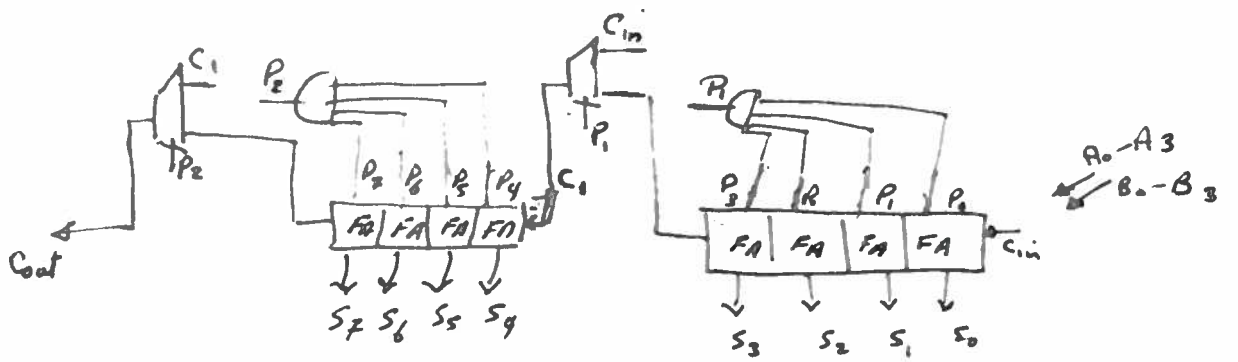
$N = 1011 \quad = 11 \quad 2N^2 + 1 = 243$



$128 + 64 + 32 + 16 + \qquad 2 + 1 \quad = 243$

Q 2

This implementation can be done on several ways, in terms of how to divide the 8-bit. Below we give implementation by using two 4-bit Carry skip Adder

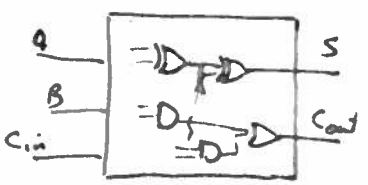


Critical Path Carry skip $= 8 * \gamma_{FA} + 2\gamma_{AND} + 2\gamma_{MUX} = 8*3 + 2\gamma_{gate} + 3*2\gamma_{gate}$
$= 32\gamma_{gate}$

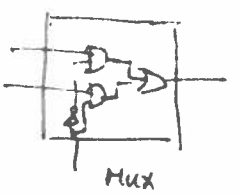
Critical Path Carry Ripple $= 8 * \gamma_{FA}$
$= 8*3 = 24\gamma_{gate}$

Area of Carry skip $= 8 * A_{FA} + 2A_{AND} + 2A_{MUX}$
$= 8*5A_{gate} + 2A_{gate} + 2*3A_{gate}$
$= 48 A_{gate}$

Area of Carry Ripple $= 8 * Area\ FA$
$= 8 * 5 A_{gate} = 40 A_{gate}$



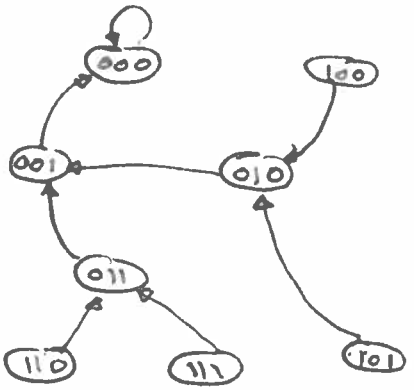
Full Adder
Delay = $3\gamma_{gate}$
Area = $5 A_{gate}$



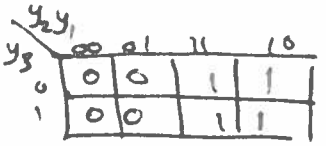
Delay $3\gamma_g$
Area $= 4\gamma_g$
neglect inverter

Q3

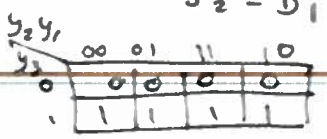
Oct 2012



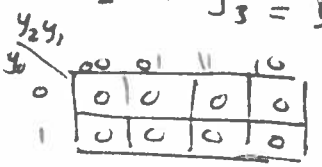
Present state			Next state		
y_3	y_2	y_1	y_3^+	y_2^+	y_1^+
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	0



$y_1^+ = y_2 = D_1$



$y_2^+ = y_3 = D_2$



$y_3^+ = 0 = D_3$

Using D Flip Flop

$y_3^+ = 0 = D_3$

$y_2^+ = y_3 = D_2$

$y_1^+ = y_2 = D_1$