EESM518 VLSI SIGNAL PROCESSING ARCHITECTURE (SPRING, 2007)

Tutorial 5: Verilog-top Mix-HDL Simulation

This tutorial will guide you to carry out the verilog simulation (including gate-level simulation) with the course provided TSMC0.25um library. For those who use VHDL language for the course project, you can just follow the tutorial 1-4 for your coding, synthesis, simulation and layout. **For those who use verilog, please do have a look at this tutorial and it is useful especially for your gate-level simulation.**

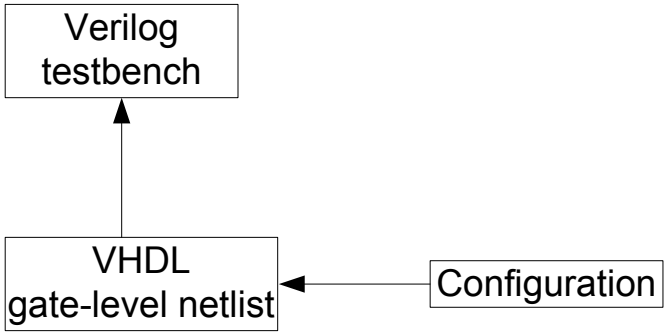
1. Write the verilog behavior code and verilog testbench for your project design. Carry out the VCS simulation to verify the function of your code.
2. Synthesis your behavior code with the synopsys tool design_analyzer. You can follow the steps in tutorial 1 for the synthesis. **Before synthesis, do check the files (including hidden files) in the folder where you invoke design_analyzer by "ls –a".**

   2 hidden files should be inside the folder with the name .synopsys_dc.setup and .synopsys_vss.setup. The 2 files can be copied from the folder */staff/ee/dept/public/elec516/template_vtvt/synopsys/**syn**/*
3. After you synthesized the design, you should save it in VHDL and verilog format separately as stated in step 27(tutorial 1) and step 1(tutorial 2). The files are the gate-level description of your synthesized design. VHDL format is for you gate-level simulation and verilog file is for your layout place and route.

   Since our provided TSMC0.25um timing library is in VHDL format, you gate-level netlist should also be in VHDL. However, your top level testbench may be in verilog. The following steps will guide you to carry out the mix-HDL simulation with the verilog testbench.

   Here, 3 files are provided for a simple example. File "mux_compiled.vhd" is the gate-level netlist description of the mux design after the synthesis. File "cfg_mux_unit.vhd" is the configuration file. File"tb_mux.v" is the verilog testbench.

   The relationship between the 3 files is shown below.



3.1. Write the configuration file for the gate-level netlist. The format is

*configuration **configuration_file_name** of **gate-level_design_entity_name** is*

*for **gate-level_design_architecture_name***

end for;

*end **configuration_file_name**;*

3.2. Go to the simulation directory. **Before simulation, check the file (including the hidden file) in the folder by "ls –a".** A file should be inside named .synopsys_vss.setup. If you don't have the file, you can copy it from the folder */staff/ee/dept/public/elec516/template_vtvt/synopsys/**sim**/*

3.3. Analyze the design and sub-design VHDL or verilog code.

If it is VHDL file, use the command

*vhdlan **your_VHDL_sub-design_name***

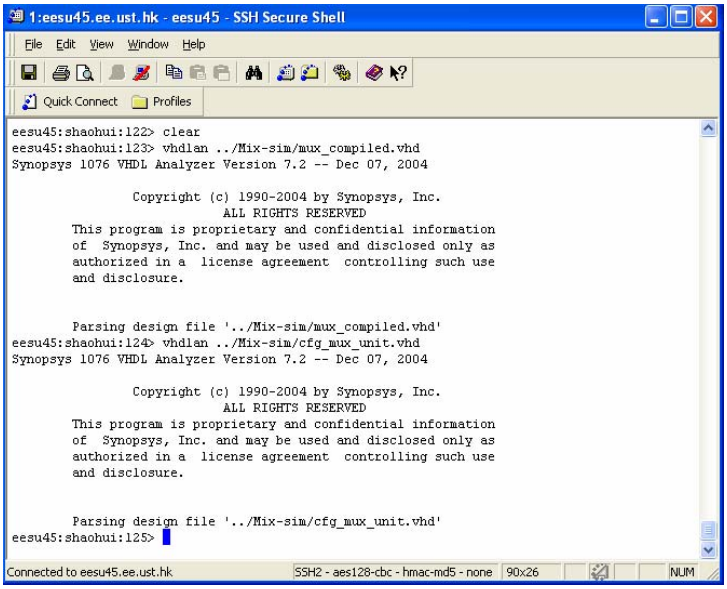
If it is verilog file, use the command

vlogan ***your_verilog_sub-design_name***

After that, analyze the configuration file

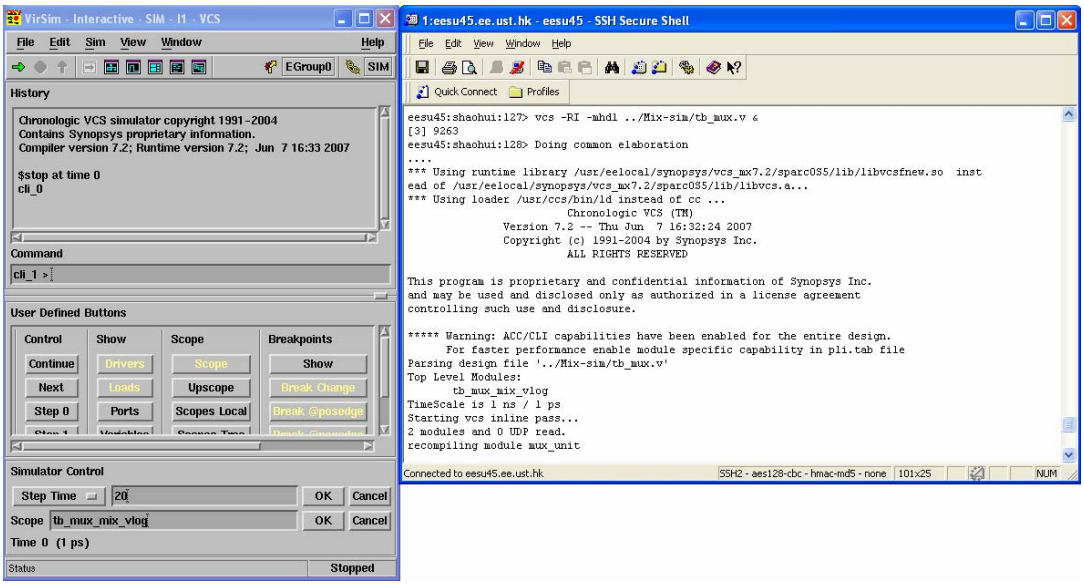
vhdlan ***configuration_file_name***

In our example, I analyzed the synthesized mux gate-level VHDL netlist and configuration file:



3.4. Use VCS to carry out the gate-level simulation with the verilog testbench by command

vcs –RI –mhdl ***verilog_testbench_name*** *&*



After that, the virsim simulation window will pop up and you can check the simulation results there.

A more complex sample design for verilog VHDL mix simulation can be found in folder

/staff/ee/dept/public/elec516/template_vtvt/synopsys/MixedHDL