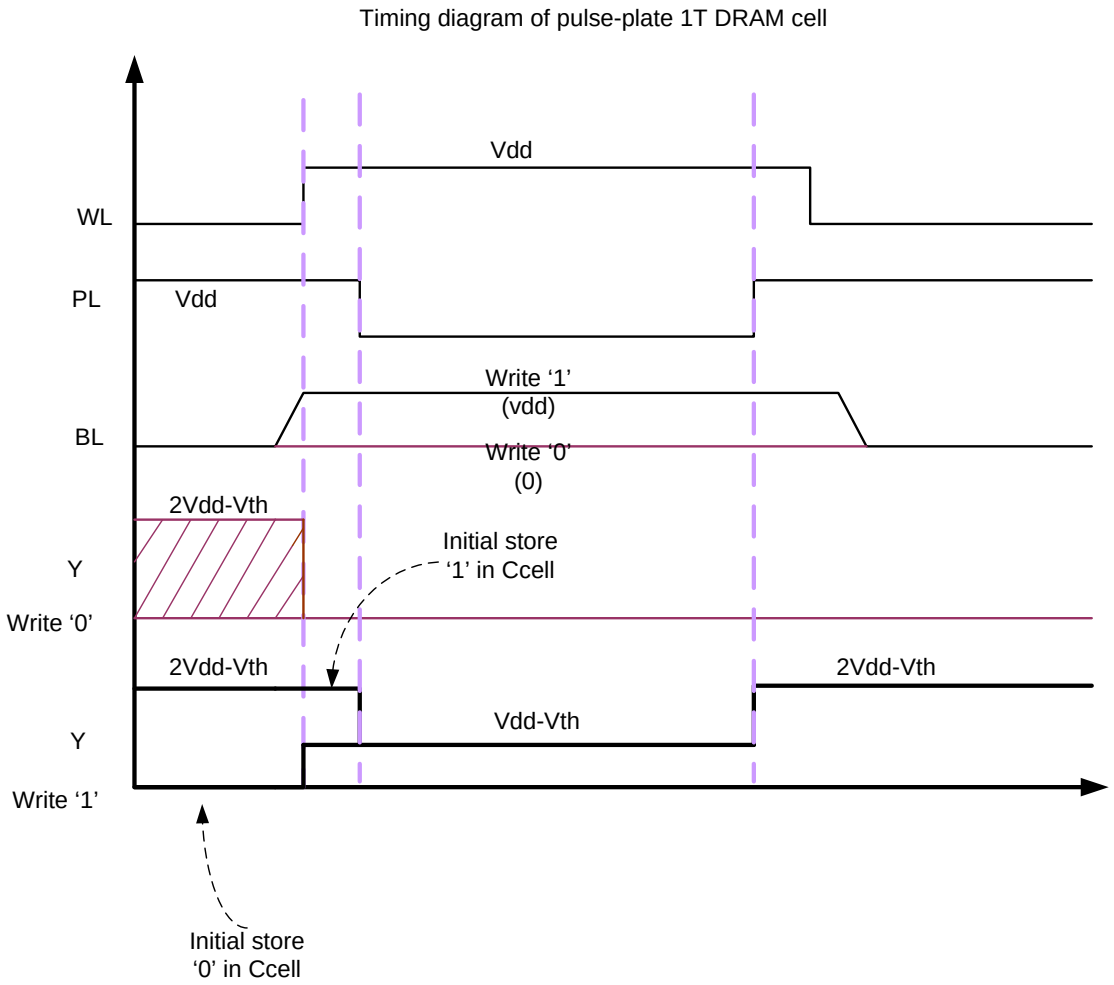
ELEC516 Digital VLSI System Design and Design Automation (spring, 2010)

Assignment 4 – Reference solution

1) Pulse-plate 1T DRAM cell

a) Timing diagrams for nodes BL and Y when writing “0” and “1”



b) From figures in (a), to store ‘0’ in this DRAM cell, voltage of node Y is 0;while writing ‘1’, this voltage changes to $2V_{dd} - V_{th}$. The voltage difference between ‘1’ and ‘0’ state increases by $(V_{dd} - V_{th})$ compared with normal 1T-DRAM architecture. The profit brought by larger voltage difference includes better noise tolerance, easier design for sense amplifier and smaller leakage etc.

c) BL is pre-discharged to 0 in read operation. When reading '0', since voltage on node Y is zero initially, after asserting WL for read operation $V_{BL} = 0$. When reading '1', from charge sharing equation, we've:

$$(2V_{dd} - V_t - V_{dd}) \times C_{cell} + 0 \times C_{BL} = C_{BL} \times V_{BL} + (V_{BL} - V_{dd}) \times C_{cell}$$

$$\Rightarrow V_{BL} = \frac{(2V_{dd} - V_{th}) \times C_{cell}}{C_{cell} + C_{BL}}$$

d) From equation in c), we can have:

$$\because \Delta V_{BL} \geq 250mV \Rightarrow C_{cell} > 13.89\,fF$$

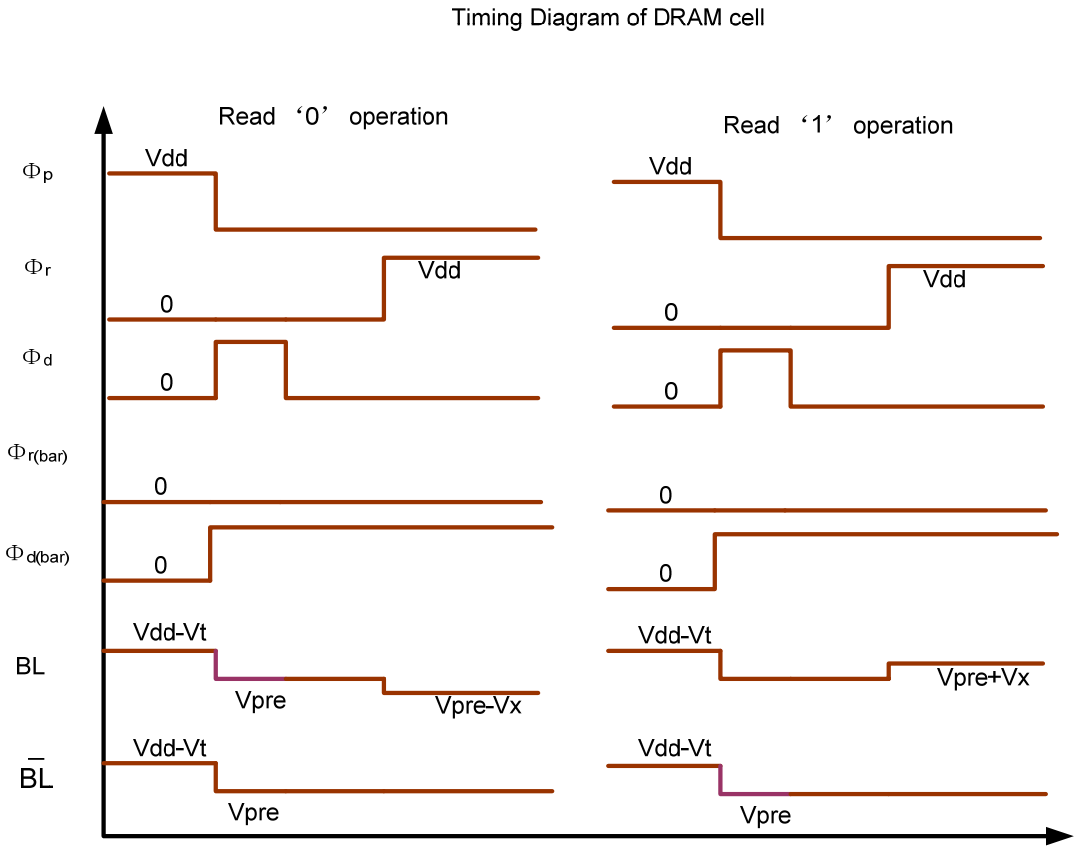
2) DRAM with divided bit-line structure

a) C_{BL} is contributed by dummy and DRAM cells as well as the input capacitance of sense amplifier (considering the pre-charge transistor also):

$$C_{bit} = 256 \times 8\,fF + 50\,fF + 2 \times 8\,fF = 2.114\,pF$$

(note: if ignoring the pre-charge transistor, $C_{bit} = 256 \times 8\,fF + 50\,fF + 8\,fF = 2.106\,pF$)

b) Timing diagram is as follows:



Normally, C_d is adopted to be close to C_{bit}, since we want to $V_{pre} = \frac{(V_{dd} - V_{th}) \times C_{bit}}{C_d + C_{bit}}$ close to $\frac{V_{dd}}{2}$.

c) From charge balance equations, for each side of sense amplifier:

$$C_{BL} \times V_{pre} + C_c \times V_{store} = (C_{BL} + C_c) \times (V_{pre} + \Delta V)$$

$$\Delta V = \frac{C_c \times (V_{store} - V_{pre})}{C_{BL} + C_c}$$

To read "0", $V_{store\_0} = 0$; to read "1", $V_{store\_1} = V_{dd} - V_{th}$;

In ideal, we want to $\Delta V_{store\_0} = \Delta V_{store\_1}$; $\therefore V_{pre} = \frac{1}{2}(V_{store\_1} - V_{store\_0}) = \frac{1}{2}(V_{dd} - V_{th})$

The voltage difference seen by sense amplifier thus can be represented as:

$$V_{BL} - V_{pre} = \frac{1}{2}\frac{C_c}{C_{BL} + C_c}(V_{dd} - V_{th}) \approx \frac{1}{2}\frac{C_c \times V_{dd}}{C_{BL} + C_c} \geq 60mV$$

$$\Rightarrow C_c \geq 51.98\,fF$$

3) Column Decoder design

Consider implementing the design using a hybrid way: (Assume pre-decode x bits)

$N_{dec} = N_{pre} + N_{pass} + N_{tree} = (x+1) \times 2^x + 2^4 + 2(2^{4-x} - 1)$;

Since the number of serial pass transistors are restricted to 3. thus x can be 2,3,4;

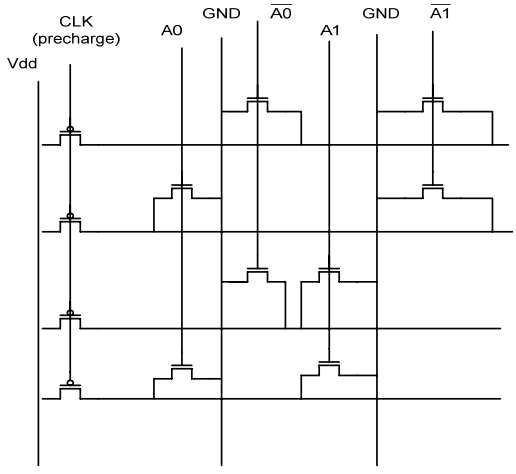
$$x = 2 \Rightarrow N_{dec} = 46$$

$$x = 3 \Rightarrow N_{dec} = 50$$

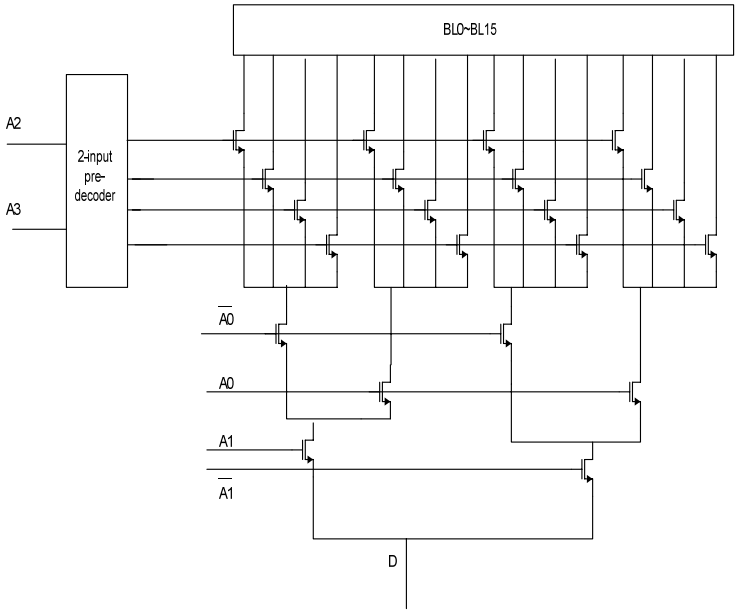
$$x = 4 \Rightarrow N_{dec} = 96$$

Thus, the most efficient implementation is pre-decoding 2 bits:

The reference schematic is as follows:

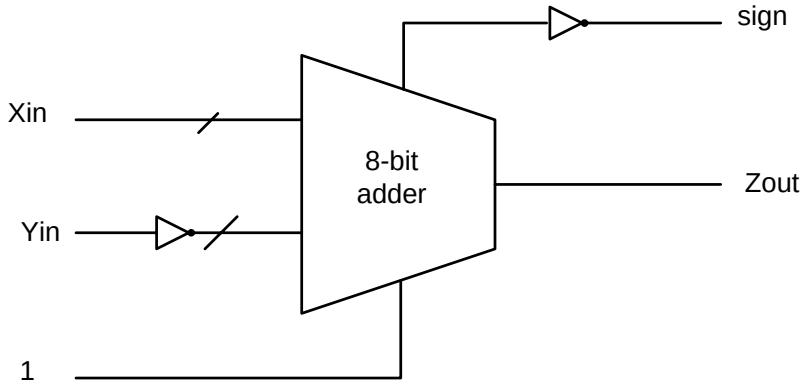


Pre-decoder

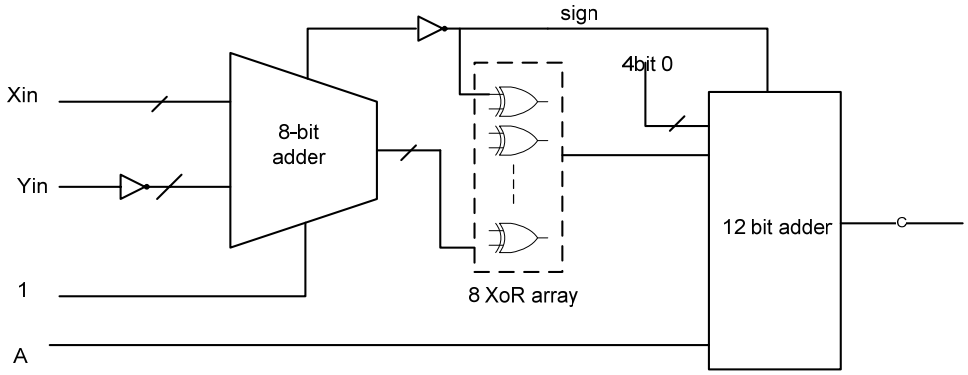


4) MSE Processing Element design

a) two's complement subtraction on 8bit data:



b) One possible design can be as follows:



Delay:

$$D = d_{inv} + d_{8bit\_adder} + d_{inv} + d_{EX-OR} + d_{12bit\_adder} = 7.6ns$$

According to timing requirement:

$T \geq T_{clk-Q} + D + T_{setup} = 0.3 + 7.6 + 0.1 = 8ns$ This corresponds to 125MHz.

c) $P_M = SC \times V^2 \times f$

d) For pipelining case, since we reduce the critical path, the maximum clock frequency can be increased. On the other hand, if we maintain the same clock frequency which corresponds to a fixed performance requirement. We can reduce the supply voltage to still meet the delay requirement. From c), by reducing supply voltage, power reduction can be obtained.

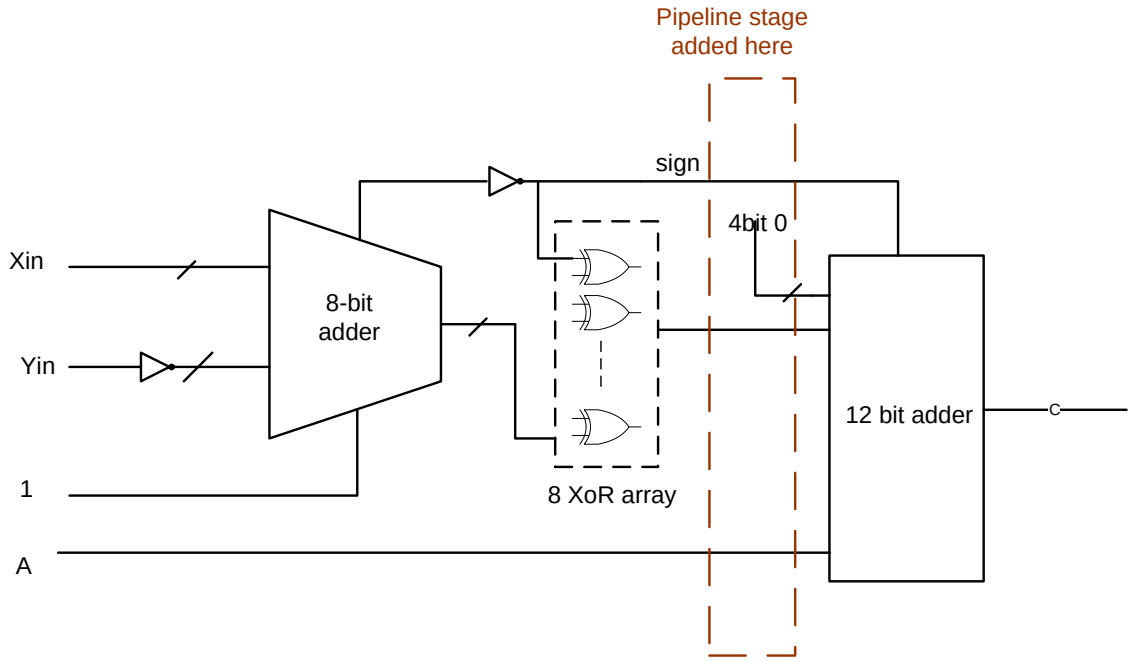
For parallel case, although *SC* increases due to duplicating some hardware in the design. The throughput also increases. For the fixed performance requirement, we can reduce clock frequency and supply voltage. From c), we can observe P_M decreases.

e) For design in b) , we have :

$P_M = (C_{8bit\_adder} + 9 \times C_{inv} + 8 \times C_{xor} + C_{12bit\_adder} + 39 \times C_{reg}) \times V^2 \times f$

$\Rightarrow P_M = (1200 + 180 + 240 + 2000 + 1560) \times 10^{-15} \times 25 \times 125 \times 10^6 = 16.2mW$

f) The new design is supposed to be as follows:



Delay in stage one is: $D_1 = t_{inv} + t_{8bit\_adder} + t_{inv} + t_{xor} = 0.4 + 2.8 + 0.4 = 3.6ns$

Delay in stage two is: $D_2 = t_{12bit\_adder} = 4ns$

Maximum clock frequency is : $T_{clk} \geq \max(D_1, D_2) + t_{setup} + t_{ck-q} = 4.4ns$

If we still want to run in 125MHz, the new voltage is :

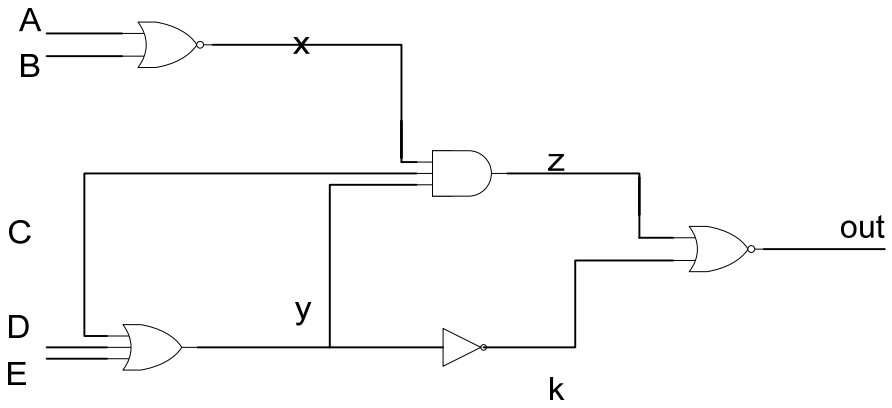
$$\frac{V_{new}}{5V} = \frac{4.4ns}{8ns} \Rightarrow V_{new} = 2.75V$$

The new power consumption thus can be formulated:

$$P_{M\_new} = SC_{new} \times V_{new}{}^2 \times f = (SC_{old} + 20 \times C_{reg}) \times V_{new}{}^2 \times f$$
$$\Rightarrow (5180 + 800) \times 2.75^2 \times 125 = 5.65mW$$

5) Design for testability

a) Test vector (X,X,0,0,0)
b) The stuck-at-1 fault of node y can also be found by same vector



6) Low Power design

a) For transition based encoding, (Assume initial state is 0000000000)

Data vector	Transition based code
0000100100	0000100100 (2 transitions)
1110101011	1110001111 (7 transitions)
0110010100	1000111111 (4 transitions)
0110100100	0000110000 (5 transitions)
0111010100	0001110000 (1 transitions)
1000101001	1111111101 (6 transitions)
0101000100	1101101101 (2 transitions)
1010011000	1111011100 (4 transitions)
1010010000	0000001000 (6 transitions)

Total number of transitions are : 37

$$E = \frac{1}{2} CV^2 \times SW = 37 \times \frac{1}{2} \times 1pf \times 1V^2 = 18.5pJ$$

b) For active high coding:
Total number of transitions are : 45

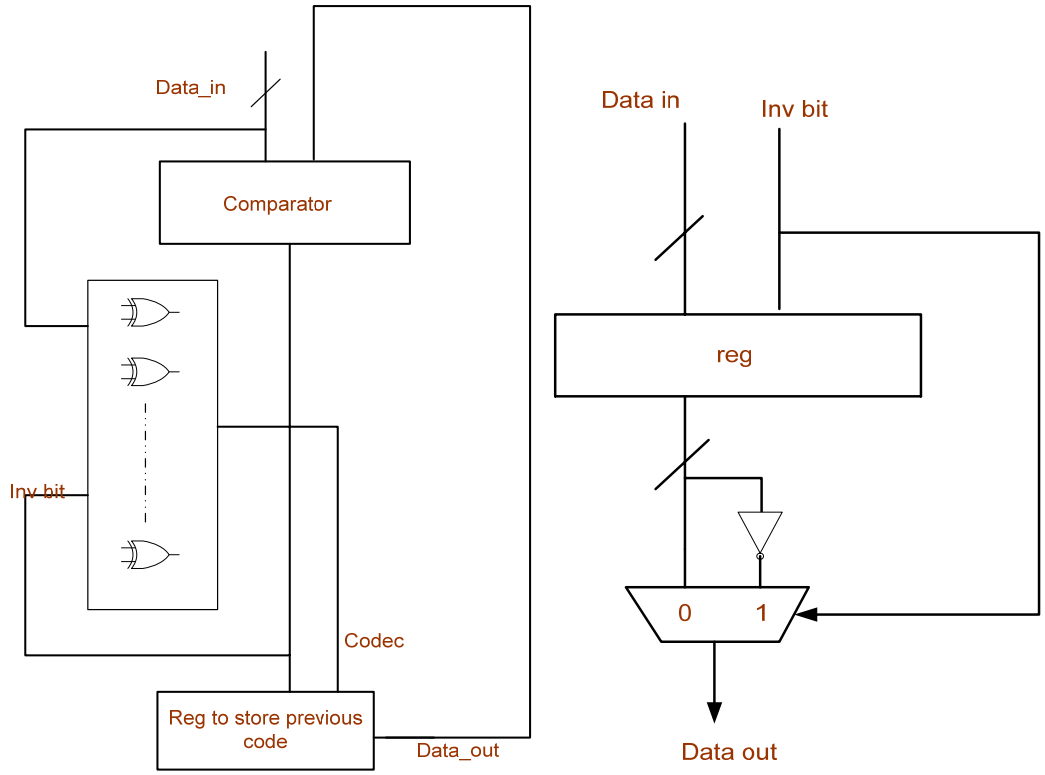
$$E = \frac{1}{2} CV^2 \times SW = 45 \times \frac{1}{2} \times 1pf \times 1V^2 = 22.5pJ$$

c) For redundant coding:

Data vector	Redundant code	Inv bit
0000100100	0000100100	0 (2 transitions)
1110101011	0001010100	1 (4 transitions)
0110010100	0110010100	0 (4 transitions)
0110100100	0110100100	0 (2 transitions)
0111010100	0111010100	0 (3 transitions)
1000101001	0111010110	1 (2 transitions)
0101000100	0101000100	0 (4 transitions)
1010011000	0101100111	1 (4 transitions)
1010010000	0101101111	1 (1 transitions)

Total number of transitions : 26 ;

$E = \frac{1}{2} CV^2 \times SW = 26 \times \frac{1}{2} \times 1pf \times 1V^2 = 13pJ$; 42.2% energy saving can be obtained



(block diagram of encoder and decoder)