INTEGRATED CIRCUITS

DATA SHEET

INTERRUPT CONTROLLER

PRODUCT SPECIFICATION

2001 Nov 23

INTERRUPTS

The XA-G3 supports 38 vectored interrupt sources. These include 9 maskable event interrupts, 7 exception interrupts, 16 trap interrupts, and 7 software interrupts.

The maskable interrupts each have 8 priority levels and may be globally and/or individually enabled or disabled.

The XA defines four types of interrupts:

- **Exception Interrupts** – These are system level errors and other very important occurrences which include stack overflow, divide-by-0, and reset.

- **Event interrupts** – These are peripheral interrupts from devices such as UARTs, timers, and external interrupt inputs.

- **Software Interrupts** – These are equivalent of hardware interrupt, but are requested only under software control.

- **Trap Interrupts** – These are TRAP instructions, generally used to call system services in a multi-tasking system.

Exception interrupts, software interrupts, and trap interrupts are generally standard for XA derivatives and are detailed in the XA User Guide.

Event interrupts tend to be different on different XA derivatives.

The XA-G3 supports a total of 9 maskable event interrupt sources (for the various XA peripherals), seven software interrupts, 5 exception interrupts (plus reset), and 16 traps. The maskable event interrupts share a global interrupt disable bit (the EA bit in the IEL register) and each also has a separate individual interrupt enable bit (in the IEL or IEH registers).

Only three bits of the IPA register values are used on the XA-G3. Each event interrupt can be set to occur at one of 8 priority levels via bits in the Interrupt Priority (IP) registers, IPA0 through IPA5. The value 0 in the IPA field gives the interrupt priority 0, in effect disabling the interrupt.

A value of 1 gives the interrupt a priority of 9, the value 2 gives priority 10, etc.

The result is the same as if all four bits were used and the top bit set for all values except 0.

Details of the priority scheme may be found in the XA User Guide.

The complete interrupt vector list for the XA-G3, including all 4 interrupt types, is shown in the following tables.

The tables include the address of the vector for each interrupt, the related priority register bits (if any), and the arbitration ranking for that interrupt source.

The arbitration ranking determines the order in which interrupts are processed if more than one interrupt of the same priority occurs simultaneously.

Interrupt Vectors

EXCEPTION/TRAPS PRECEDENCE

DESCRIPTION	VECTOR ADDRESS	ARBITRATION RANKING
Reset (h/w, watchdog, s/w)	0000-0003	0 (High)
Breakpoint (h/w trap 1)	0004-0007	1
Trace (h/w trap2)	0008-000B	1
Stack Overflow (h/w trap3)	000C-000F	1
Divide by 0 (h/w trap4)	0010-0013	1
User RETI (h/w trap5)	0014-0017	1
TRAP 0-15 (software)	0040-007F	1

EVENT INTERRUPTS

DESCRIPTION	FLAG BIT	VECTOR ADDRESS	ENABLE BIT	INTERRUPT PRIORITY	ARBITRATION RANKING
External interrupt 0	IE0	0080-0083	EX0	IPA0.2-0	2
Timer 0 interrupt	TF0	0084-0087	ET0	IPA0.6-4	3
External interrupt 1	IE1	0088-008B	EX1	IPA1.2-0	4
Timer 1 interrupt	TF1	008C-008F	ET1	IPA1.6-4	5
Timer 2 interrupt	TF2(EXF2)	0090-0093	ET2	IPA2.2-0	6
Serial port 0 Rx	RI.0	00A0-00A3	ERI0	IPA4.6-4	7
Serial port 0 Tx	TI.0	00A4-00A7	ETI0	IPA4.2-0	8
Serial port 1 Rx	RI.1	00A8-00AB	ERI1	IPA5.6-4	9
Serial port 1 Tx	TI.1	00AC-00AF	ETI1	IPA5.2-0	10

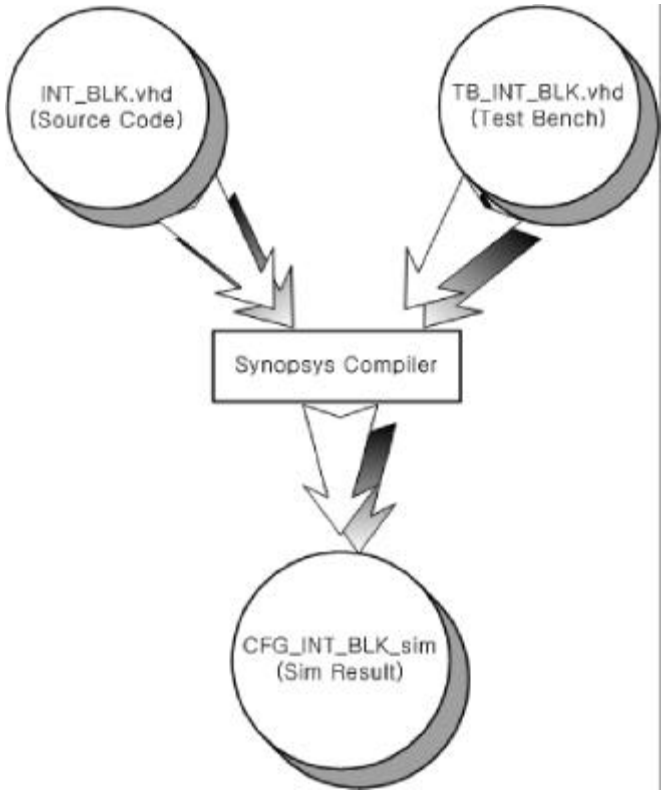
SOFTWARE INTERRUPTS

DESCRIPTION	FLAG BIT	VECTOR ADDRESS	ENABLE BIT	INTERRUPT PRIORITY
Software interrupt 1	SWR1	0100-0103	SWE1	(fixed at 1)
Software interrupt 2	SWR2	0104-0107	SWE2	(fixed at 2)
Software interrupt 3	SWR3	0108-010B	SWE3	(fixed at 3)
Software interrupt 4	SWR4	010C-010F	SWE4	(fixed at 4)
Software interrupt 5	SWR5	0110-0113	SWE5	(fixed at 5)
Software interrupt 6	SWR6	0114-0117	SWE6	(fixed at 6)
Software interrupt 7	SWR7	0118-011B	SWE7	(fixed at 7)

Pin Description

Pin Name	Type	Description
clock	Input	main clock pin
reset	Input	main reset pin
ir_en	Input	interrupt enable pin
start_reg_en	Input	interrupt start register enable pin
icall_start	Input	interrupt routine call start pin
intrpt_reset	Input	interrupt reset pin
intrpt_trace	Input	interrupt trace pin
intrpt_stack_ov	Input	interrupt stack overflow pin
intrpt_div_0	Input	interrupt divide pin
intrpt_reti	Input	interrupt routine return pin
intrpt_event	Input	interrupt event vector pin
intrpt_swr	Input	interrupt SWR register pin
ea	Input	enable pin
ei_enable	Input	interrupt enable vector pin
swe	Input	interrupt SWE register pin
current_priority	Input	currunt state priority pin
ipa0_low	Input	IPA0 low register pin
ipa0_high	Input	IPA0 high register pin
ipa1_low	Input	IPA1 low register pin
ipa1_high	Input	IPA1 high register pin
ipa2_low	Input	IPA2 low register pin
ipa4_low	Input	IPA4 low register pin
ipa4_high	Input	IPA4 high register pin
ipa5_low	Input	IPA5 low register pin
ipa5_high	Input	IPA5 high register pin
rst_ext0	Output	external0 interrupt reset pin
rst_ext1	Output	external1 interrupt reset pin
rst_timer0	Output	timer0 interrupt reset pin
rst_timer1	Output	timer1 interrupt reset pin
intrpt_rdy_start	Output	interrupt ready pin
real_intrpt_rdy	Output	real interrupt ready pin
real_intrpt_addres	Output	real interrupt address bus

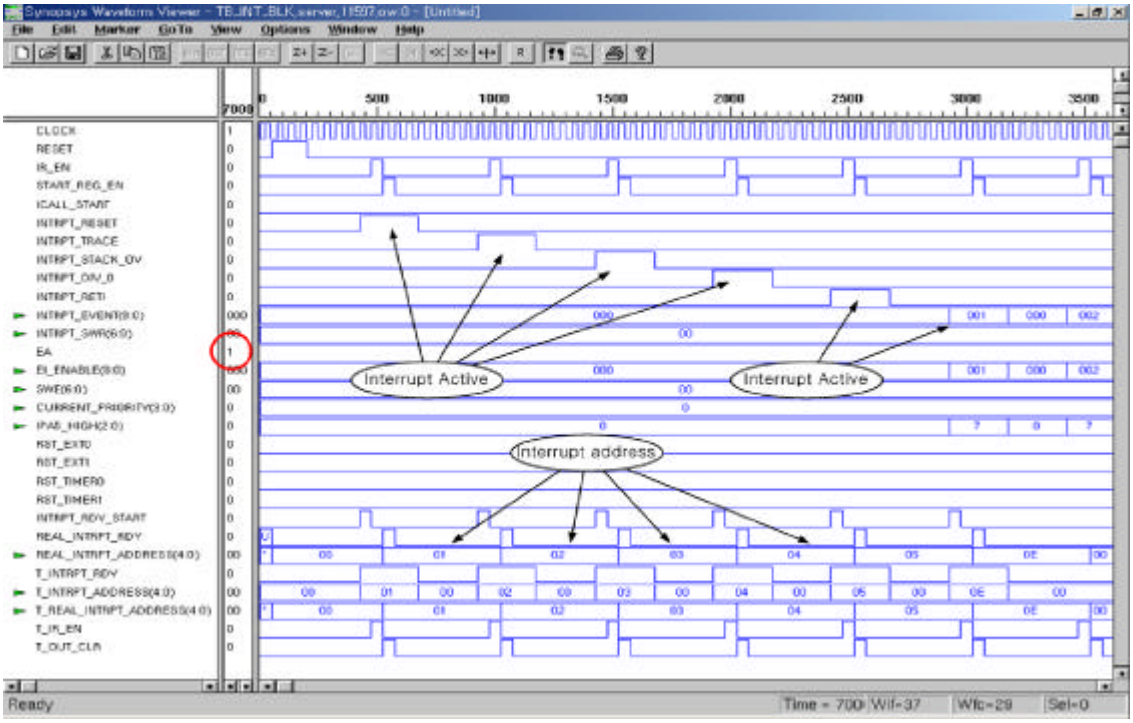
Prototype method



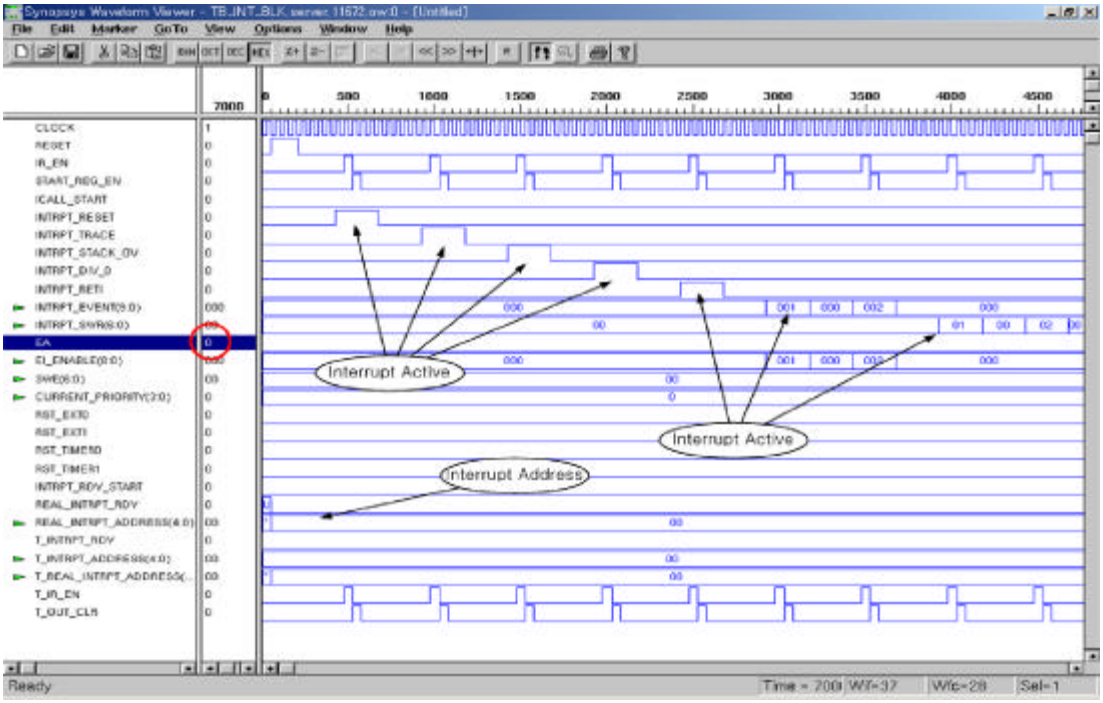
int_blk.vhd and tb_int_blk.vhd compile to verified simulation result file (cfg_int_blk_sim).

※ Compiler Tool : Synopsys Compiler

Result Simulation



Interrupt Controller execution result - branch ISR routine



Interrupt Controller execution result - not execution ISR routine