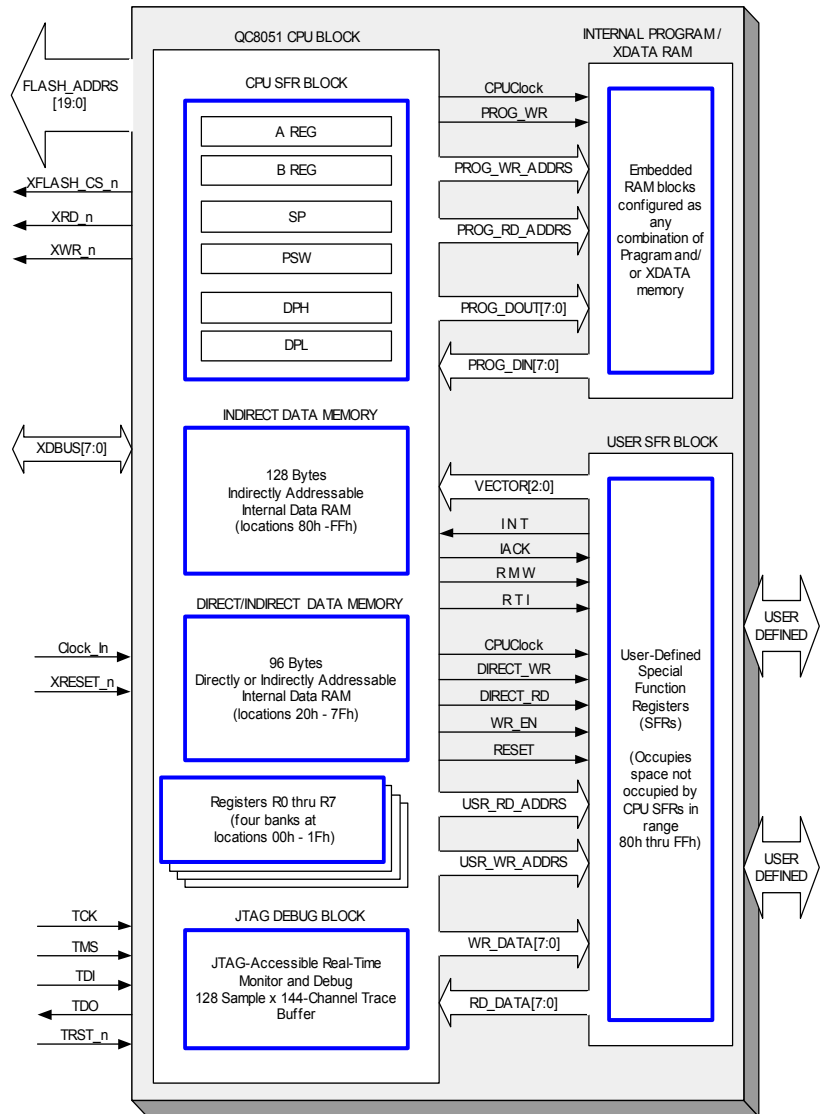


Features and Benefits

- ❑ Implement custom 8051 designs in an Actel ProASIC^{PLUS} FPGA using Actel Libero Development Environment Software and QuickCores QC8051 Real-Time Development Kit
- ❑ Compatible with Keil Software μ Vision2** debugger and C compiler
- ❑ Includes QuickCores small memory model (2K program reach) synthesizable QC8051 netlist library (compatible with Libero)
- ❑ Includes BoxView*** real-time "C" language debugger for QuickCores QC8051
- ❑ Includes target board with Actel APA-300 installed
- ❑ Flash-USB+ APA Device Programmer/Debugger (included in kit) :
 - Programs the Actel APA device
 - JTAG boundary scan controller (SAMPLE/PRELOAD monitoring)
 - JTAG real-time monitor/debugger interface
- ❑ 256KB (150ns) external flash memory for program/data storage
- ❑ 2-line X 16 character LCD
- ❑ 4 user buttons & 8 user LEDs
- ❑ RS-232 interface for user applications
- ❑ QuickCores QC8051 features:
 - Pipeline architecture allows most instructions execute in a single clock cycle
 - Customizable user SFR block
 - Real-time monitor architecture allows monitoring of internal operations without the use of embedded software routines via JTAG connection
 - Debug logic includes 128-sample deep X 144-channel real-time trace buffer
 - Traces 36-bit time stamp, PC, Instruction Register, PSW, SP, ACC, B, DP, Data RD address/data, Data WR address/data, interrupt acknowledge
 - Unlimited software breakpoints
 - Up to three hardware breakpoints



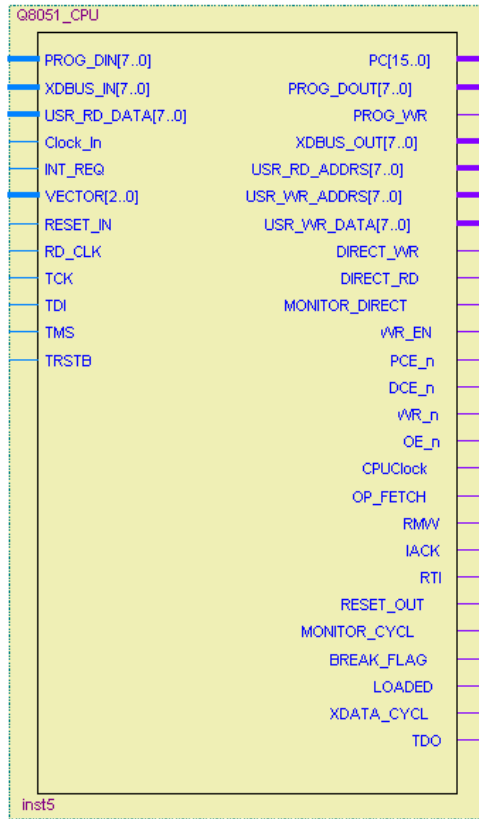
General Description

When used with Actel Libero integrated design environment software, QuickCores FPGA-8051 Real-Time Development Kit allows you to quickly create and debug custom 8051 designs in an Actel ProASIC^{PLUS} FPGA. The kit includes QuickCores small memory model QC8051 softcore, BoxView C language debugger which is compatible Keil Software 8051 C compiler and μ Vision2 IDE, target board and power supply. Example top-level 8051 references design programming files are also included. Large memory model QC8051 netlist library is available under a separate license.

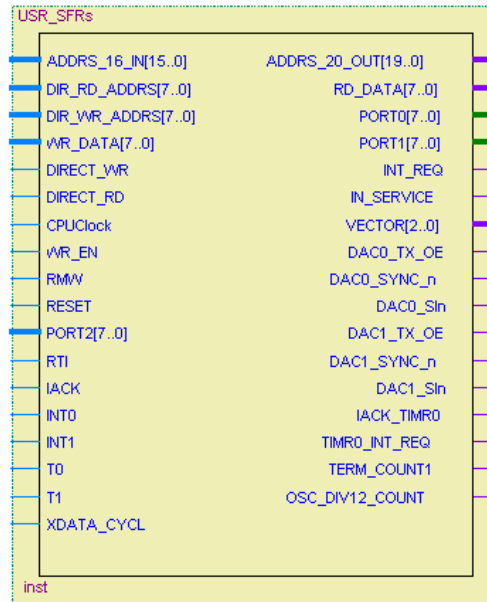
QC8051 CPU Module Signal Descriptions (instantiated at top level of your design)

Name	Dir	Description
PROG_DIN[7:0]	I	QC8051 program instruction bus input
PROG_DOUT[7:0]	O	QC8051 program write bus used by real-time monitor program write cycles
PROG_WR	O	Indicates program write during real-time monitor program write cycles
XDBUS_IN[7:0]	I	QC8051 external data bus input
XDBUS_OUT[7:0]	O	QC8051 external data bus output
PCE_n	O	Active low external program memory chip enable
DCE_n	O	Active low external data memory chip enable
OE_n	O	Active low external program/data output enable
WR_n	O	Active low external program/data write enable
USR_RD_ADDRS[7:0]	O	User SFR read address
USR_WR_ADDRS[7:0]	O	User SFR write address
USR_RD_DATA[7:0]	I	User SFR read data bus
USR_WR_DATA[7:0]	O	User SFR write data bus
DIRECT_WR	O	1 = internal data memory "direct" write cycle
DIRECT_RD	O	1 = internal data memory "direct" read cycle
MONITOR_DIRECT	O	1 = internal monitor data memory direct read cycle
WR_EN	O	1 = internal data memory write enable
Clock_In	I	External clock input
CPUClock	O	CPU clock output
MODE	I	1 = CPU clock = Clock_In / 1; 0 = CPU clock = Clock_In / 4 (use this for external interfacing)
OP_FETCH	O	1 = opcode fetch cycle
RMW	O	1 = read-modify-write cycle
IACK	O	1 = interrupt acknowledge cycle
INT_REQ	I	1 = interrupt request
VECTOR[2:0]	I	Bits [5:3] of the interrupt vector loaded into the program counter
RESET_IN	I	1 = reset
RESET_OUT	O	1 = reset; this signal internally gated by JTAG debug module
MONITOR_CYCL	O	1 = monitor cycle
XDATA_CYCL	O	1 = MOVX instruction; used by memory expansion circuit
TCK	I	JTAG TCK input
TDI	I	JTAG TDI input
TMS	I	JTAG TMS input
TRST_n	I	JTAG TRST_n input
TDO	O	JTAG TDO output

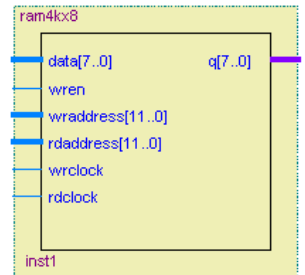
FPGA-8051 Real-Time Development Kit Netlist Library Top-Level Instantiation Symbols



Q8051 CPU (2K Memory Model)

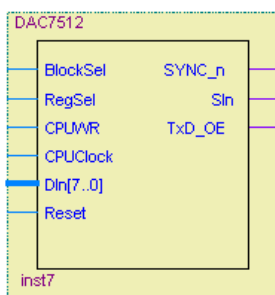


User-Definable SFR Block

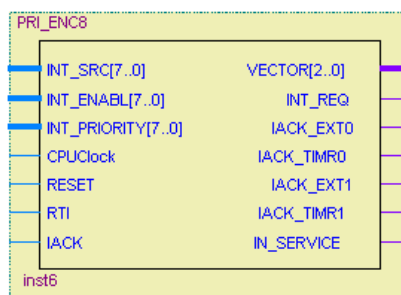


Various Size RAM Blocks for Program / Data Storage

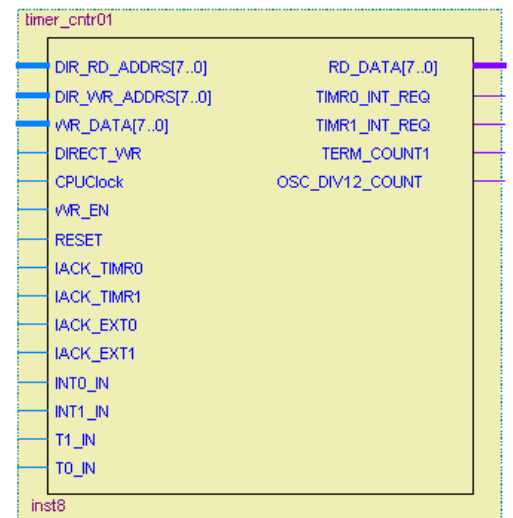
User-Definable Special Function Register Block Symbols Included in FPGA-8051 Netlist Library



DAC7512 Serial Controller Port



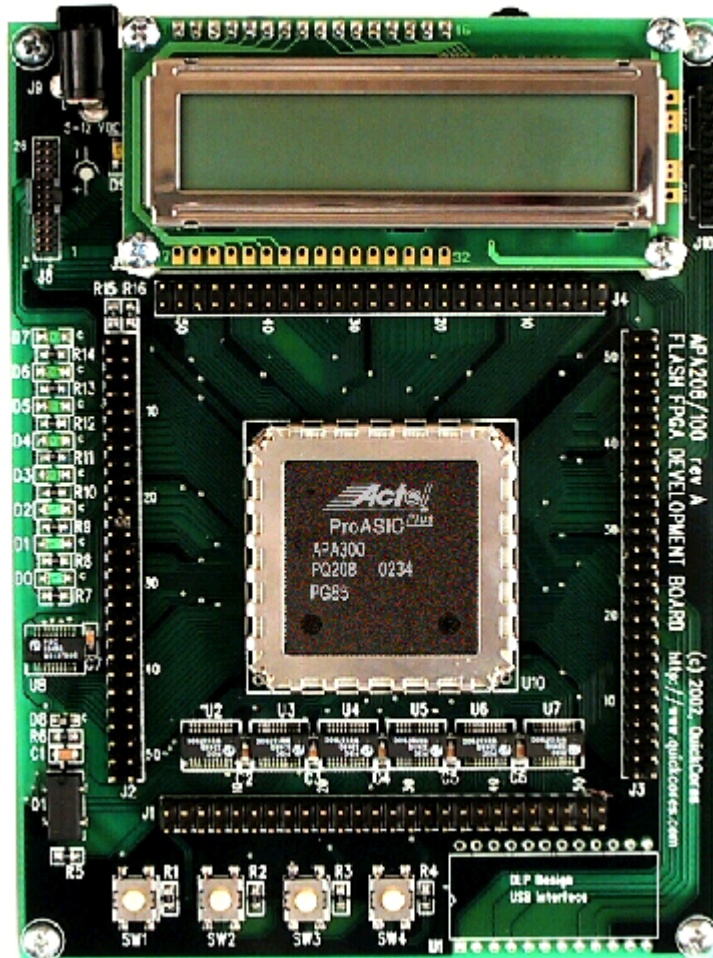
Interrupt Controller Block



Dual 16-Bit Counter/ Timer Module

Note: Other modules not shown include general purpose parallel port and external program / data memory extended address banking module. Large Memory Model Q8051 CPU and serial port available under separate license.

QuickCores APA-208 Target Board



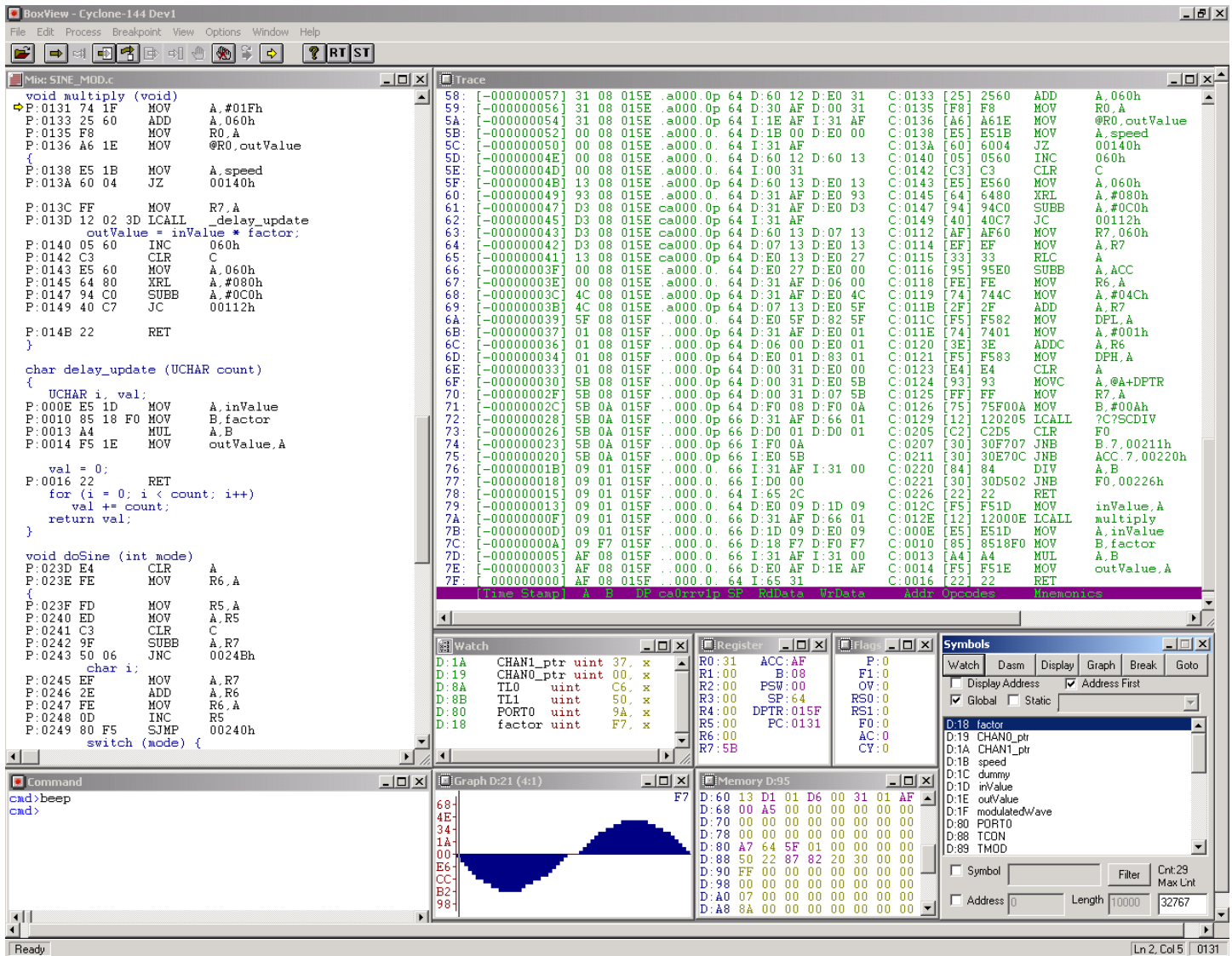
ProASIC^{PLUS} APA208 Target Board Description

The QuickCores FPGA-8051 Real-Time Development Kit for Actel ProASIC^{PLUS} FPGAs includes the APA208 Target Board pictured above. Programming the flash-based ProASIC^{PLUS} device is through the FlashUSB+ programming/debug pod included in the kit. Once the device is programmed with the desired QC8051 design, the implemented QC8051 design user application software can be programmed and debugged using the same FlashUSB+ pod. JTAG boundary scan (SAMPLE/PRELOAD) monitoring of the ProASIC^{PLUS} APA device pins is also by way of the FlashUSB+ pod interface.

Provided on the APA208 Target Board for your use are 128 Kbytes (x16 bits) external flash memory, 2-line X 16-character LCD, four user buttons and 12.288 MHz oscillator.

Although the QuickCores QC8051 Real-Time Development Kit includes an Actel APA-300 ProASIC^{PLUS} FPGA, small (2k-reach) memory model QC8051 netlist library which you can use to create your own designs, the APA208 Target Board is shipped with a large memory model QC8051 programmed into the ProASIC^{PLUS} APA device and on CD.

BoxView C Language Real-Time Debugger

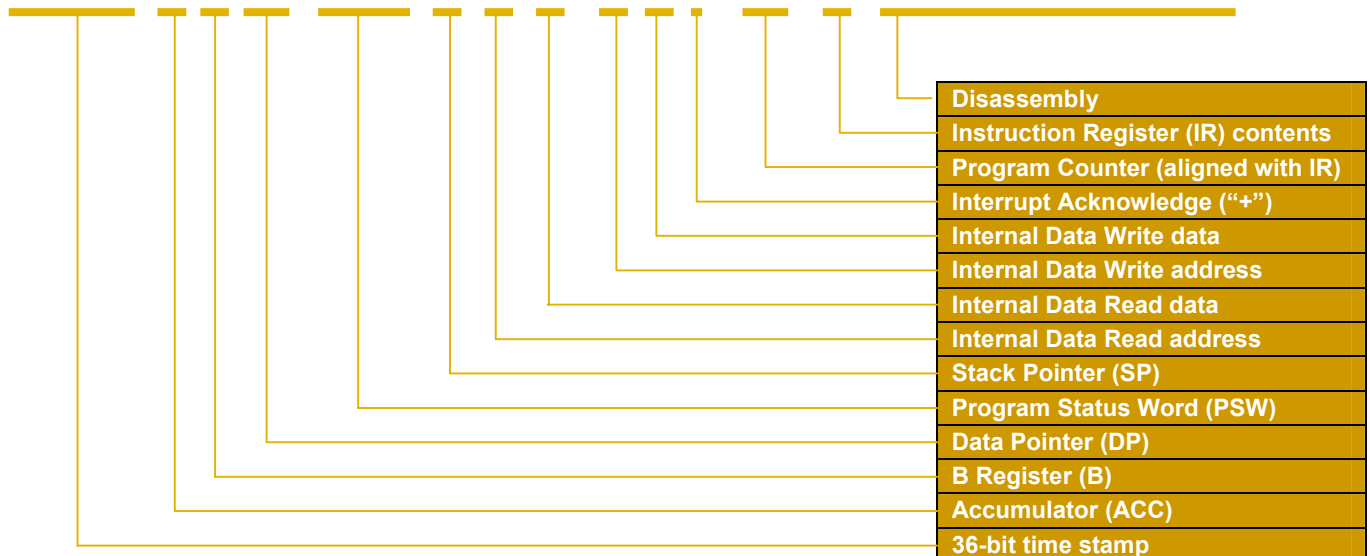


BoxView Real-Time C Language Debugger Key Features

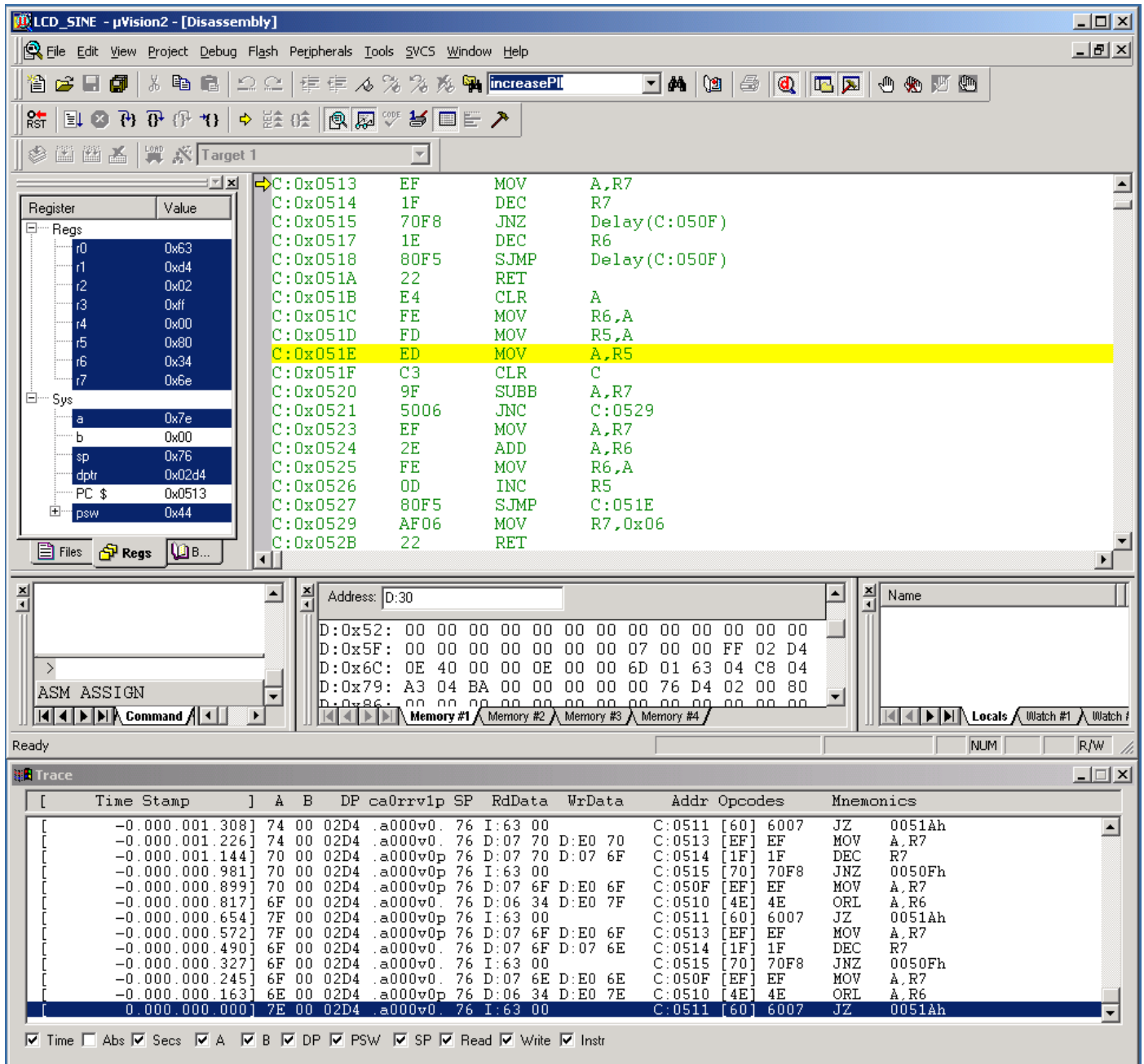
- Built-in STAPL player programs the target APA device via QuickCores Flash-232+ or Flash-USB+ pod.
- Real-time trace buffer displays 36-bit time stamp, ACC, B, DP, PSW, SP, Data RD address and data, Data WR address and data, PC and Instruction Register contents
- Supports concurrent and remote monitoring and debugging of multiple CPUs
- Code window with source, mixed or assembly display mode
- “Symbols” widow allows you to quickly set breakpoints, disassemble, or watch
- Multiple memory windows for data, code, indirect, or external locations
- Graphic display of any memory region allows animation in real-time mode
- On-the-fly monitoring and editing of registers and memory
- Robust JTAG command and scripting language with data logging for automated testing

FPGA-8051 Debug Module 128 Sample X 144-Channel Real-Time Trace Buffer

Time Stamp	A	B	DP	ca0rrvlp	SP	RdData	VrData	Addr	OpCodes	Mnemonic
57: [-000000059]	19	00	0164	ca000.0p	64	D:E0	19 D:E0	33	C:0115 [33]	33 RLC A
58: [-000000057]	00	00	0164	.a000.0.	64	D:E0	33 D:E0	00	C:0116 [95]	95E0 SUBB A,ACC
59: [-000000056]	00	00	0164	.a000.0.	64	D:37	06 D:06	00	C:0118 [FE]	FE MOV R6,A
5A: [-000000054]	4C	00	0164	.a000.0p	64	D:37	06 D:E0	4C	C:0119 [74]	744C MOV A,#04Ch
5B: [-000000053]	4C	00	0164	.a000.0p	64	D:07	19 D:E0	65	C:011B [2F]	2F ADD A,R7
5C: [-000000051]	65	00	0165	.a000.0.	64	D:E0	65 D:82	65	C:011C [F5]	F582 MOV DPL,A
5D: [-00000004F]	01	00	0165	.a000.0p	64	D:37	06 D:E0	01	C:011E [74]	7401 MOV A,#001h
5E: [-00000004E]	01	00	0165	.a000.0p	64	D:06	00 D:E0	01	C:0120 [3E]	3E ADDC A,R6
5F: [-00000004C]	01	00	0165	.0000.0p	64	D:E0	01 D:83	01	C:0121 [F5]	F583 MOV DPH,A
60: [-00000004B]	01	00	0165	.0000.0p	64	D:00	37 D:E0	00	C:0123 [E4]	E4 CLR A
61: [-000000048]	00	00	0165	.0000.0.	66	D:00	37 D:66	01 +	C:0124 [93]	93 MOVC A,@A+DPTR
62: [-000000045]	00	00	0165	.0000.0.	66	I:37	06		C:000B [02]	02018C LJMP 0018Ch
63: [-000000043]	00	00	0165	.0000.0.	67	D:E0	00 D:67	00	C:018C [C0]	C0E0 PUSH ACC
64: [-000000041]	00	00	0165	.0000.0.	68	D:D0	00 D:68	00	C:018E [C0]	C0D0 PUSH PSW
65: [-00000003E]	00	00	0165	.001.0.	68	D:D0	00 D:D0	08	C:0190 [75]	75D008 MOV PSW,#008h
66: [-00000003C]	00	00	0165	.001.0.	68	D:A8	8A D:A8	0A	C:0193 [C2]	C2AF CLR IE.7
67: [-00000003A]	1F	00	0165	.001.0p	68	D:2F	09 D:E0	1F	C:0195 [74]	741F MOV A,#01Fh
68: [-000000038]	30	00	0165	.a001.0.	68	D:19	11 D:E0	30	C:0197 [25]	2519 ADD A,019h
69: [-000000037]	30	00	0165	.a001.0.	68	D:2F	09 D:08	30	C:0199 [F8]	F8 MOV R0,A
6A: [-000000036]	30	00	0165	.a001.0.	68	D:30	09 D:E0	09	C:019A [E6]	E6 MOV A,@R0
6B: [-000000034]	89	00	0165	.a001.0p	68	D:30	09 D:E0	89	C:019B [64]	6480 XRL A,#080h
6C: [-000000032]	89	00	0165	.a001.0p	68	D:E0	89 D:9D	89	C:019D [F5]	F59D MOV 09Dh,A
6D: [-000000030]	89	00	0165	.a001.0p	68	D:19	11 D:19	12	C:019F [05]	0519 INC 019h
6E: [-00000002E]	12	00	0165	.a001.0.	68	D:19	12 D:E0	12	C:01A1 [E5]	E519 MOV A,019h
6F: [-00000002B]	12	00	0165	ca001.0.	68	I:30	09		C:01A3 [B4]	B44003 CJNE A,#040h,001A
70: [-000000029]	12	00	0165	ca001.0.	68	D:1C	01 D:1C	02	C:01A9 [05]	051C INC 01Ch
71: [-000000027]	02	00	0165	ca001.0p	68	D:1C	02 D:E0	02	C:01AB [E5]	E51C MOV A,01Ch
72: [-000000024]	02	00	0165	ca001.0p	68	I:30	09		C:01AD [B4]	B41005 CJNE A,#010h,001B
73: [-000000022]	02	00	0165	ca001.0p	68	D:A8	0A D:A8	8A	C:01B5 [D2]	D2AF SETB IE.7
74: [-000000020]	02	00	0165	.0000.0p	67	D:68	00 D:D0	00	C:01B7 [D0]	D0D0 POP PSW
75: [-00000001E]	00	00	0165	.0000.0.	66	D:67	00 D:E0	00	C:01B9 [D0]	D0E0 POP ACC
76: [-00000001B]	00	00	0165	.0000.0.	64	I:65	24		C:01BB [32]	32 RETI
77: [-000000018]	3C	00	0165	.0000.0.	64	D:00	37 D:E0	3C	C:0124 [93]	93 MOVC A,@A+DPTR
78: [-000000017]	3C	00	0165	.0000.0.	64	D:00	37 D:07	3C	C:0125 [FF]	FF MOV R7,A
79: [-000000014]	3C	0A	0165	.0000.0.	64	D:F0	00 D:F0	0A	C:0126 [75]	75F00A MOV B,#00Ah
7A: [-000000010]	3C	0A	0165	.0000.0.	66	D:37	06 D:66	01	C:0129 [12]	120205 LCALL 00205h
7B: [-00000000E]	3C	0A	0165	.0000.0.	66	D:D0	00 D:D0	00	C:0205 [C2]	C2D5 CLR F0
7C: [-00000000B]	3C	0A	0165	.0000.0.	66	I:F0	0A		C:0207 [30]	30F707 JNB B.7,00211h
7D: [-000000008]	3C	0A	0165	.0000.0.	66	I:E0	3C		C:0211 [30]	30E70C JNB ACC.7,00220h
7E: [-000000003]	06	00	0165	.0000.0.	66	I:37	06 I:37	00	C:0220 [84]	84 DIV A,B
7F: [000000000]	06	00	0165	.0000.0.	66	I:D0	00		C:0221 [30]	30D502 JNB F0,00226h



Keil Software μ Vision2 IDE Supports QuickCores FPGA-8051 Soft Core



The screenshot displays the Keil Software μ Vision2 IDE interface for disassembling the LCD_SINE program. The main window shows the following assembly code:

```

C:0x0513 EF MOV A,R7
C:0x0514 1F DEC R7
C:0x0515 70F8 JNZ Delay(C:050F)
C:0x0517 1E DEC R6
C:0x0518 80F5 SJMP Delay(C:050F)
C:0x051A 22 RET
C:0x051B E4 CLR A
C:0x051C FE MOV R6,A
C:0x051D FD MOV R5,A
C:0x051E ED MOV A,R5
C:0x051F C3 CLR C
C:0x0520 9F SUBB A,R7
C:0x0521 5006 JNC C:0529
C:0x0523 EF MOV A,R7
C:0x0524 2E ADD A,R6
C:0x0525 FE MOV R6,A
C:0x0526 0D INC R5
C:0x0527 80F5 SJMP C:051E
C:0x0529 AF06 MOV R7,0x06
C:0x052B 22 RET
    
```

The left pane shows the Register window with the following values:

Register	Value
r0	0x63
r1	0xd4
r2	0x02
r3	0xf
r4	0x00
r5	0x80
r6	0x34
r7	0x6e

The bottom pane shows the Trace window with the following data:

Time Stamp	A	B	DP	ca0rrvip	SP	RdData	WrData	Addr	Opcodes	Mnemonics
-0.000.001.308]	74	00	02D4	.a000v0	76	I:63 00		C:0511 [60]	6007	JZ 0051Ah
-0.000.001.226]	74	00	02D4	.a000v0	76	D:07 70	D:E0 70	C:0513 [EF]	EF	MOV A,R7
-0.000.001.144]	70	00	02D4	.a000v0p	76	D:07 70	D:07 6F	C:0514 [1F]	1F	DEC R7
-0.000.000.981]	70	00	02D4	.a000v0p	76	I:63 00		C:0515 [70]	70F8	JNZ 0050Fh
-0.000.000.899]	70	00	02D4	.a000v0p	76	D:07 6F	D:E0 6F	C:050F [EF]	EF	MOV A,R7
-0.000.000.817]	6F	00	02D4	.a000v0	76	D:06 34	D:E0 7F	C:0510 [4E]	4E	ORL A,R6
-0.000.000.654]	7F	00	02D4	.a000v0p	76	I:63 00		C:0511 [60]	6007	JZ 0051Ah
-0.000.000.572]	7F	00	02D4	.a000v0p	76	D:07 6F	D:E0 6F	C:0513 [EF]	EF	MOV A,R7
-0.000.000.490]	6F	00	02D4	.a000v0	76	D:07 6F	D:07 6E	C:0514 [1F]	1F	DEC R7
-0.000.000.327]	6F	00	02D4	.a000v0	76	I:63 00		C:0515 [70]	70F8	JNZ 0050Fh
-0.000.000.245]	6F	00	02D4	.a000v0	76	D:07 6E	D:E0 6E	C:050F [EF]	EF	MOV A,R7
-0.000.000.163]	6E	00	02D4	.a000v0p	76	D:06 34	D:E0 7E	C:0510 [4E]	4E	ORL A,R6
0.000.000.000]	7E	00	02D4	.a000v0	76	I:63 00		C:0511 [60]	6007	JZ 0051Ah

Keil Software μ Vision2 IDE Key Points

- Provided with the FPGA-8051 Real-Time Development Kit are the appropriate .dlls which will allow seamless operation with Keil Software μ Vision2 IDE and C51 compiler
- Concurrent real-time monitoring and debug of multiple CPUs is supported when μ Vision2 IDE is used in combination with Domain Technologies BoxServer and BoxView Debugger
- The FPGA-8051 real-time trace buffer is supported under μ Vision2 “Peripherals” menu item

FPGA-8051 Real-Time Development Kit for ProASIC^{PLUS} Contents

The FPGA-8051 Real-Time Development Kit for ProASIC^{PLUS} comes with the following items:

- QuickCores APA-208 target board with APA-300 ProASIC^{PLUS} FPGA installed and preprogrammed with large memory model QuickCores FPGA-8051 microcontroller
- BoxView real-time C language debugger with integral STAPL player device programmer/driver
- QuickCores small (2k program reach) memory model netlist library targeted Actel ProASIC^{PLUS} FPGAs and restricted for use with Libero
- Flash-USB+ APA device programmer/debug pod
- 9-volt power supply
- Target board schematics
- User Guide
- Example large memory model FPGA-8051 top-level and user SFR designs in Verilog and compiled .rpd file format
- Required dlls for use with Keil Software μ Vision2 IDE

QuickCores Design Services

Along with its microcontroller IP, QuickCores also offers non-recurring engineering (NRE) design services to assist customers with integrating QuickCores microcontroller IP into their designs. This service is available on a quotation basis. Other services include development of custom application software, both on the host PC side and on the target embedded application side.

Ordering Information

FPGA-8051 Real-Time Development Kit part number (small memory model): **QC8051-RTDK-APA-S**

Contact Information:

QuickCores IP
811 E. Plano Parkway, Suite 115
Plano, Texas 75074
Tel: (972) 578 1121
Fax: (972) 578 1086
Email: sales@quickcores.com



Discount Coupon



Purchase a QuickCores QC8051 Real-time Development Kit (small memory model) before December 1, 2003 and receive 25% off the list price of \$595.

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