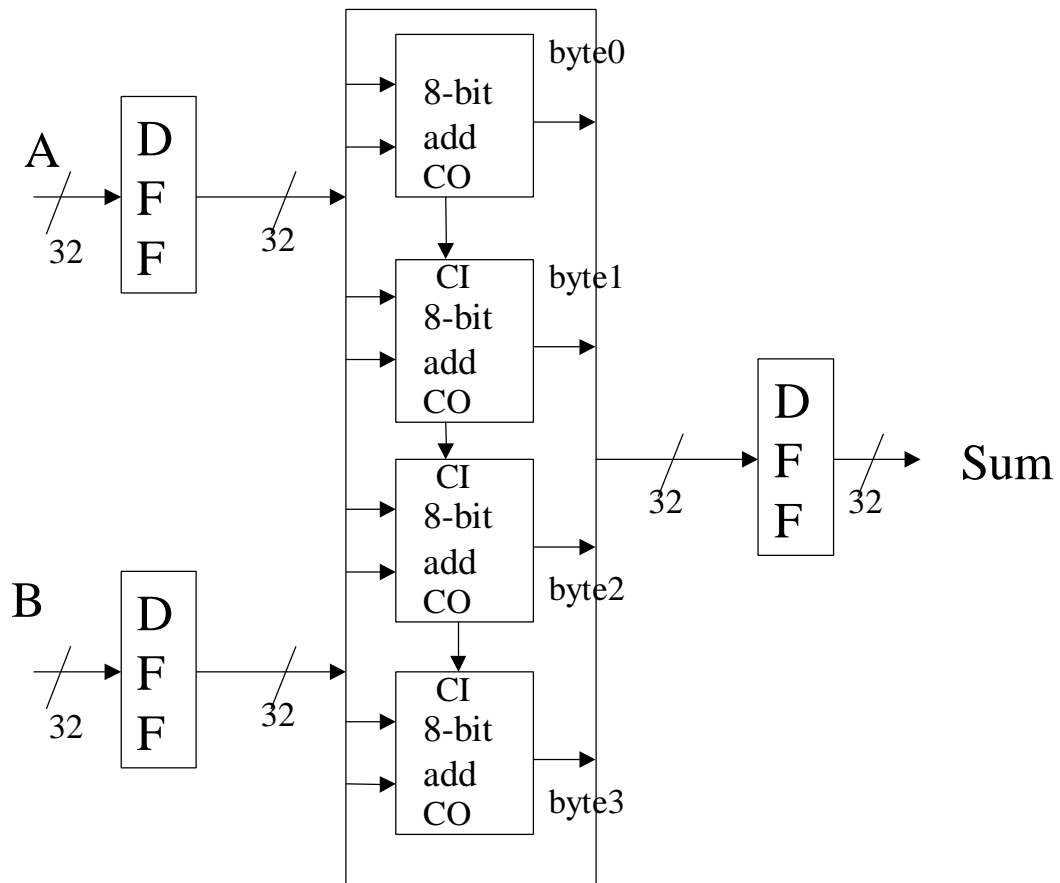


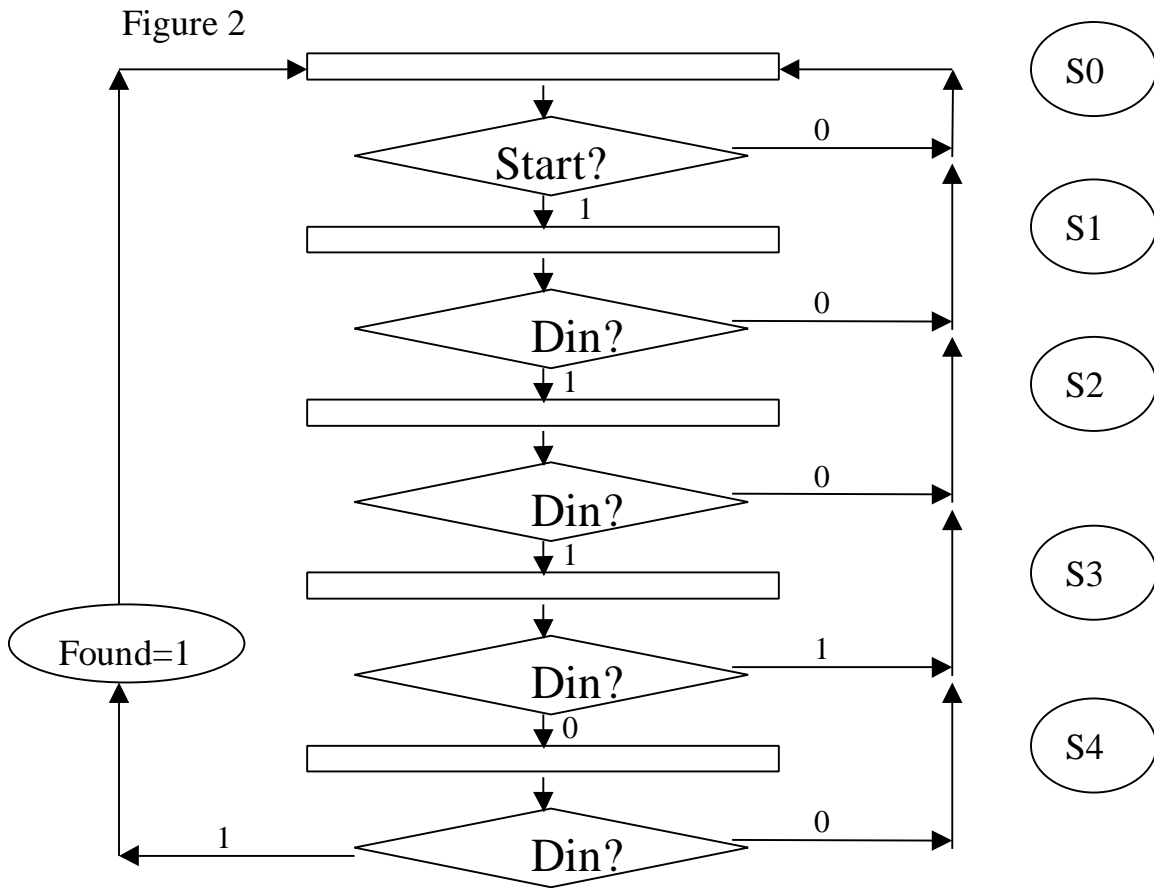
3. For the ASM chart shown in Figure 2, write the VHDL architecture block that will implement this ASM.

ARCHITECTURE a OF detector is

4. For the logic diagram shown in Figure 3, give the delays of the following paths
 - a. Longest Clock to Out
 - b. Longest Register to Register Delay
 - c. Longest Pin to Pin delay (combinational delay path).



32 Bit Ripple Carry Adder - Figure 1



Start, Din single bit inputs. Detects a serial bit sequence “1101”.

Figure 3

