Simultaneously Switching Output Limits for Actel FPGAs

Introduction

For high performance field programmable gate arrays (FPGAs) with many I/Os, the allowable number of Simultaneously Switching Outputs (SSOs) for each device is an important issue for system designers. The limits for SSOs depend on factors such as package type and die size. Use the following guidelines to help ensure reliable system designs.

System Noise and Transients

Noise generated by off-chip drivers is a major concern in FPGA design for high-performance systems. Noise is closely related to interconnections and increases as a function of fast rise times, large total chip currents and die dimensions, and small spacing between components on-chip and onboard. As clock frequencies and die dimensions increase, signal wavelengths become comparable to wire lengths, thereby making better antennas. Reduction in the spacing between circuits leads to an increase in the capacitive, inductive, and resistive couplings. The voltage (IR) drop across the power lines becomes more significant as the current densities increase and the feature size decreases. With larger amounts of current switching, the inductive noise associated with the power lines also increases. These current transients may generate large potential drops because of the inductance of the power distribution network and is referred to as simultaneous switching (ΔI) noise.

When several circuits switch simultaneously, the current supplied by the power lines can change at a very fast rate and the inductive voltage drop along the line can cause the power supply level to fall. This voltage drop is proportional to the switching speed, the number of drivers switching simultaneously, and the effective inductance of the power lines. This effect can be summarized by Faraday's Law, which states that any change in the magnetic flux will be confronted by an opposition, a self induced EMF, determined by the rate of change in the total magnetic flux, represented by this equation:

$$EMF = d\Phi/dt = LdI/dt$$

This reduction in the supply level diminishes the current drive of a circuit, increases the delay, and may lead to the spurious switching of the receiver.

SSO Recommendations

Actel defines SSOs as any outputs that transition in phase within a 10-ns window. The output current of these drivers is shown in device data sheets. The amplitude and duration of the ground bounce is a function of the number of outputs switching simultaneously and the capacitive loading of the outputs.

Table 1 shows the recommended SSO limits for Actel FPGAs. These may vary because the amount of ground bounce that an application can tolerate is difficult to determine. Worst-case conditions are simulated by placing the I/Os adjacent to each other while driving 20 pF, 35 pF, and 50 pF loads. The observed ground bounce is less than 1.5 V, with a pulse width of less than 2.0 ns. This is within the acceptable limits of the dynamic threshold of 74F, 74LS, and ACT (Advanced CMOS Technology) families. Results from the EDN Special Report on Ground Bounce Tests by David Shear[1] show a plot of the ground bounce pulse amplitude versus pulse width duration (ns) for different logic families. This article shows that as the input pulse width gets shorter, the voltage must be higher to affect the output of the device. Exceeding the recommended limits may result in larger ground bounce. The output drivers should be placed separately if more outputs must be switched simultaneously. This arrangement reduces the mutual inductance produced between adjacent I/Os resulting in a lower ground bounce. If necessary, buffers may also be inserted in the path before the output buffer. This will reduce the probability of adjacent drivers switching within 10 ns of each other.

References:

1. David Shear, "EDN Special Report on Ground Bounce Tests," *EDN*, April 15, 1993, p. 120–134.

© 1996 Actel Corporation

Table 1 • *Recommended SSO Limits for Actel FPGAs*

		Maximum Recommended SSOs for Loads		
Device	**Package**	**20 pf**	**35 pf**	**50 pf**
A1010A/A1020A	44 PLCC	40	22	16
A1010A/1020A	68 PLCC	60	34	24
A1020A	84 PLCC	80	45	32
A1010A/1020A	84 PGA	80	45	32
A1010A/A1020A	100 PQFP	80	45	32
A1280/A1280XL	PG 176, PQ 160	160	90	64
A1240/A1240XL	PG 132, PQ 144	120	68	48
A1240/A1225/A1225XL	84 PLCC	80	45	32
A1225/A1225XL	100 PGA, PQFP	80	45	32
A1400 Family[1]	84 PLCC	64	48	42
A1400 Family[1]	All other packages	128	64	58

Note:

1. The recommended SSO value for the A1400 family can be doubled for outputs using low slew drivers.