IEEE Standard 1149.1 (JTAG) in the 3200DX Family

Introduction

Due to the increasing complexity of circuit boards, testing loaded boards is becoming prohibitively expensive and more difficult to perform. Board complexity has resulted from the rapid development of surface-mount technology and from the use of multilayered boards. Finer pin spacing and the use of double-sided boards also have contributed to the increased cost and difficulty of traditional testing, which makes use of methods such as in-circuit testing by bed-of-nails and functional testing. Although functional testing can cope with complex and dense boards, it is costly because different designs require different sets of test programs.

A new method of testing reduces the cost and difficulty of board-level testing. The new standard was proposed and developed by the Joint Test Action Group (JTAG) and later adopted by IEEE as the *IEEE Standard Test Access Port and Boundary-Scan Architecture* also referred to as *IEEE Std. 1149.1* or informally as *JTAG*.

The standard provides a cost-effective method of board testing through use of the boundary-scan technique. Boundary scan provides the means to test each component's required performance, interconnections, and interaction. In addition to describing boundary scan, the standard also describes the design-for-test feature.

Overview

The Actel 3200DX family is fully compliant with the IEEE Standard 1149.1. Figure 1 shows the major parts that make up the JTAG test logic circuit. The circuit provides the required components (Test Access Port (TAP) controller and registers) to support all the mandatory boundary-scan instructions (EXTEST, SAMPLE/PRELOAD, BYPASS) and two optional instructions (HIGHZ and CLAMP). The JTAG test logic circuit also supports two private instructions, USER INSTRUCTION, and JPROBE.

JTAG Activation

The JTAG test logic circuit is activated in the Designer Series software by selecting Options/Set Die & Package. This brings up the Device Selection dialog box as shown in Figure 2. Click the Restrict JTAG Pins check box and then click the OK button. During device programming a special fuse called the *J-Fuse* is programmed, enabling the JTAG test logic circuit. The JTAG test logic circuit can also be activated when using the Actel Script language by adding the command:

Set ("RESTRICTJTAGPINS", "YES");

Test Access Port (TAP)

Each test logic function is accessed through the Test Access Port. There are four pins associated with the TAP, and they are listed in Table 1 with their corresponding descriptions. These pins are dedicated pins, which are used only with the test logic. If JTAG is not enabled, the TAP ports (TMS, TCK, and TDI) are free to be used as a regular I/O. The test logic has been designed to be in the reset state upon power-up.

Table 1 • *Test Access Port*

Port	Description
TCK (Test Clock Input)	Dedicated test logic clock used serially to shift test instruction, test data, and control inputs on the rising edge of the clock, and serially to shift the output data on the falling edge of the clock.
TMS (Test Mode Select)	Serial input for the test logic control bits. Data is captured on the rising edge of the test logic clock. This pin is equipped with a pull-up resistor to place the test logic in the Reset state when no input is present.
TDI (Test Data Input)	Serial input for instruction and test data. Data is captured on the rising edge of the test logic clock. This pin is equipped with a pull-up resistor.
TDO (Test Data Output)	Serial output for test instruction and data from the test logic. TDO is set to an Inactive Drive state (high impedance) when data scanning is not in progress.

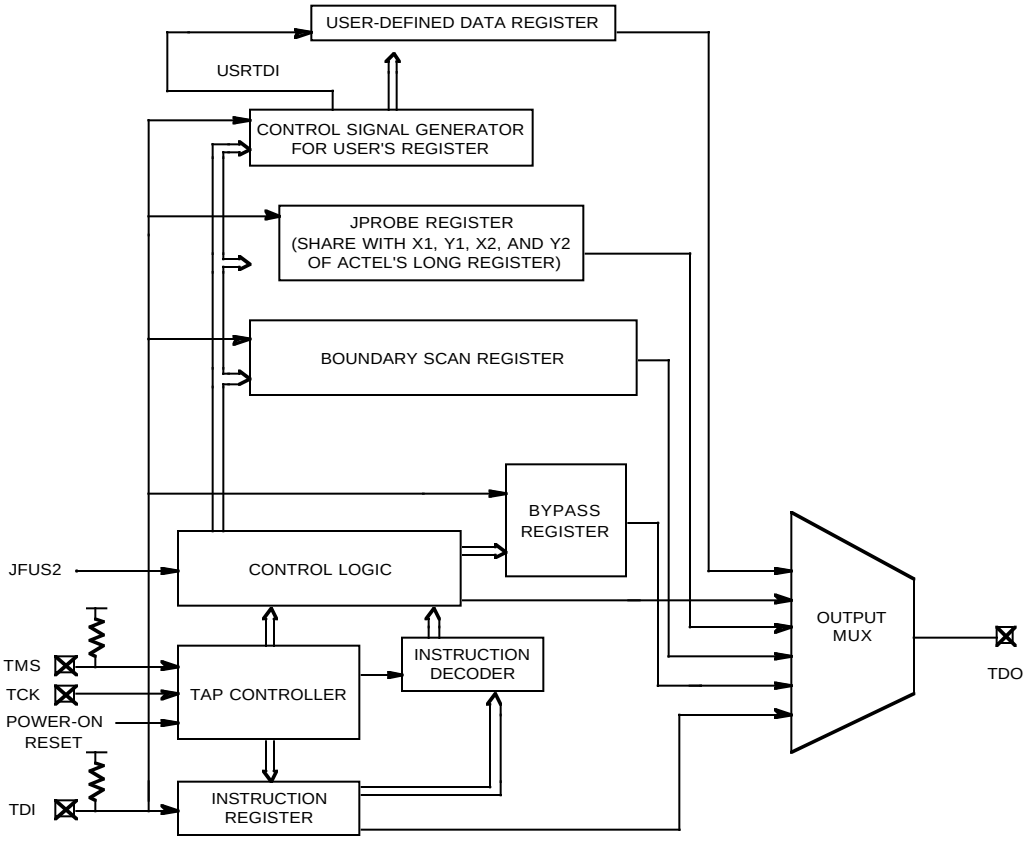


Figure 1 • *JTAG Block Diagram*

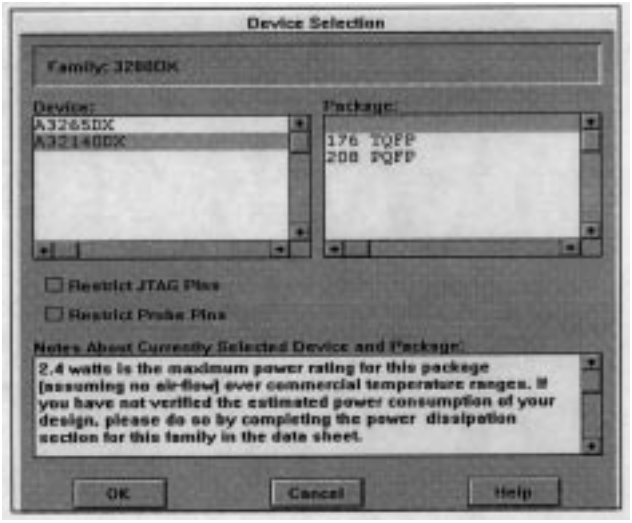
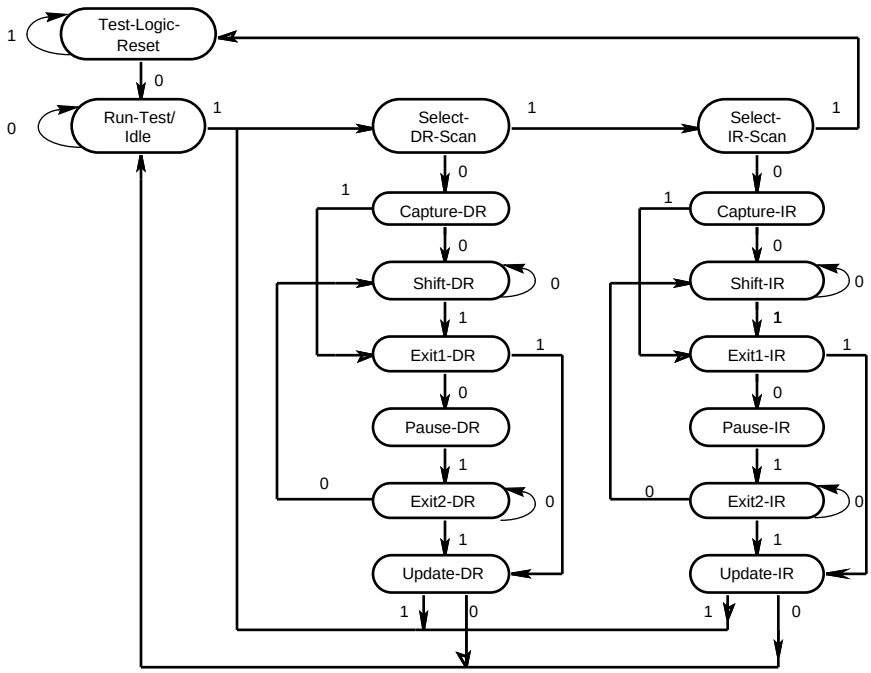


Figure 2 • *Device Selection Dialog Box*

TAP Controller

The TAP controller is a 16-state state machine that performs according to the state diagram shown in Figure 3. The 1's and 0's shown adjacent to the state transitions represent the TMS values that must be present at the time of a rising edge at TCK for a state transition to occur. In the states that include the letters -IR, the instruction register operates; in the states that contain the letters -DR, the test data register operates (bypass, boundary-scan, and JPROBE registers).



Note: *The value shown adjacent to the state transitions in this figure represents the signal present at TMS at the time of the rising edge at TCK.*

Figure 3 • *TAP Controller State Diagram*

The TAP controller receives two control inputs, TMS and TCK, and generates control and clock signals for the rest of the test logic architecture, as illustrated in Figure 4. The TAP controller's state changes based on the value of TMS, and at the rising edge of TCK or on power-up. Upon power-up, the TAP controller enters the Test-Logic Reset state. Since the TMS pin is equipped with a pull-up resistor, the TAP controller will remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be high for at least five TCK cycles.

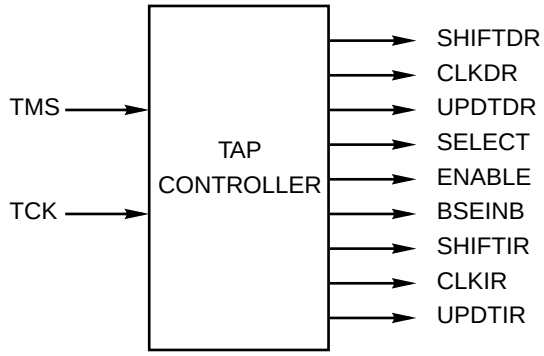


Figure 4 • *TAP Controller Block Diagram*

Instruction Register

The instruction register (IR) consists of three IR cells. Each cell has a shift-register stage and a latch stage (Figure 5). On the Capture-IR state, the shift register is loaded with bits 001, which are used for fault isolation of the board-level serial test data path. The TDI-IR-TDO path is established on the Shift-IR state. Data in the shift register is shifted toward TDO, and data in the latch remains the same. The data in the shift registers is latched out and becomes the current instruction on the falling edge of the TCK in the Update-IR state. When the TAP controller enters the Test-Logic Reset state, bits 111 are latched in IR, which corresponds to the BYPASS instruction, and the data in the shift register cell retain their previous values. Table 2 shows the summary of the operation of the instruction register.

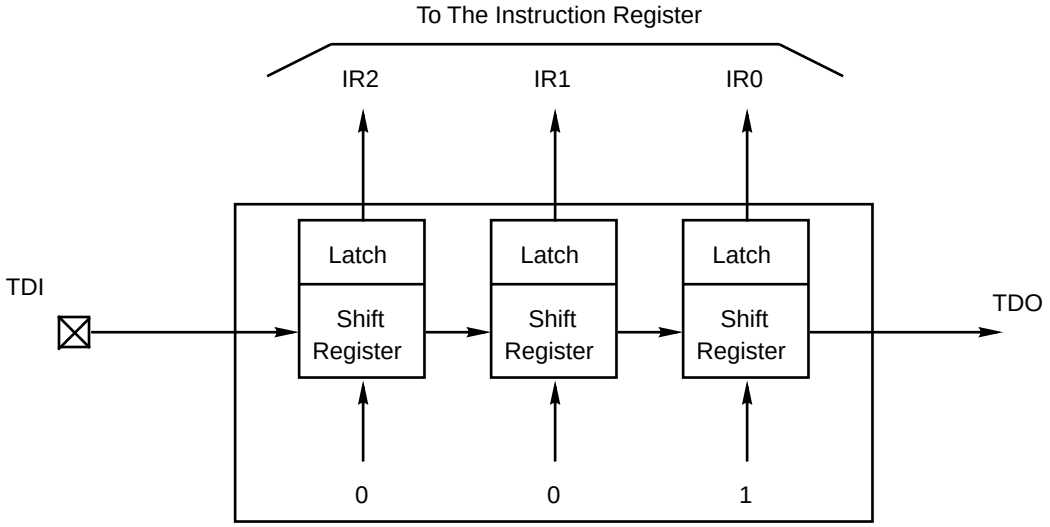


Figure 5 • *Instruction Register Block Diagram*

Table 2 • *Instruction Register Operation*

Controller State	Shift-Register Stage	Latch Stage
Test-Logic-Reset	Undefined	BYPASS Instruction IR2 IR1 IRO = 1 1 1
Capture-IR	001 is loaded	Retain previous state
Shift-IR	Shift data toward TDO	Retain previous state
Exit1-IR Exit2-IR Pause-IR	Retain previous state	Retain previous state
Update-IR	Retain previous state	Latch data from the shift register
All other states	Undefined	Retain previous state

Instructions

Table 3 lists the supported instructions with their corresponding IR codes and descriptions.

Bypass Register

The bypass register is a single-bit register that provides a minimum data path between the TDI and TDO pins (Figure 6). The bypass register is selected when the BYPASS, HIGHZ, or CLAMP instruction is the current instruction in the instruction register.

On the Capture-DR controller state, 0 is loaded into the bypass register. Test data can then be shifted from the TDI to the TDO pin on the Shift-DR state. By moving into the Update-DR controller state, data movement through the bypass register is terminated. Table 4 shows the summary of the operation of the bypass register.

Table 4 • *Bypass Register Operation*

Controller State	Bypass Register
Test-Logic-Reset	Retain previous state
Capture-DR	0 is loaded
Shift-DR	Shift data toward TDO
Exit1-DR Exit2-DR Pause-DR	Retain previous state
Update-DR	Retain previous state
All other states	Undefined

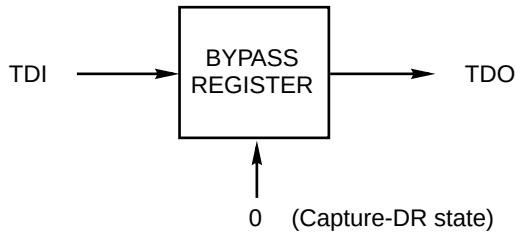


Figure 6 • *Bypass Register Block Diagram*

Table 3 • *Supported Instructions*

Instruction	IR Code = (IR2 IR1 IR0) Instruction Type	Description
EXTEST	(000) Mandatory	Permits board-level interconnect testing by applying specific test data at the output pins to the external interconnection and capturing the test result at the input pins.
SAMPLE/PRELOAD	(001) Mandatory	Used to capture data from the input pins and to apply test data into the latched parallel outputs of the boundary-scan register while the on-chip system logic is in normal operation.
JPROBE	(011) Private	Permits access to Actel's probe register for system logic signal probing.
USER INSTRUCTION	(100) Reserved	Permits access to the application-specific test data register designed by the user with Actel's logic modules.
HIGHZ	(101) Optional	Used to place the component's system logic outputs into an inactive drive state—high-impedance state.
CLAMP	(110) Optional	Permits the use of data in the boundary-scan register to be driven from component pins while the bypass register is selected as the serial path between TDI and TDO.
BYPASS	(111) Mandatory	Permits access to the single-bit shift register data path between the TDI and TDO pins to facilitate rapid movement of data through a component when the component does not require test operation.

Boundary-Scan Register

The boundary-scan register is used to observe and control the state of each system pin, including the clock pins. Each boundary-scan cell consists of serial input (SI) and serial output (SO) that are connected to each cell, as shown in Figure 7. In addition, each cell consists of a parallel input (PI) and a latched parallel output (PO) that connect to the system logic and system output. Three cells are used for each I/O: an input cell (BS2), an output cell (BS1), and an output-enable cell (BS0).

The operation of the boundary-scan register under specific boundary-scan instruction is illustrated in Tables 5 and 6.

If the EXTEST instruction is not being used in conjunction with the SAMPLE/PRELOAD instruction, the external test starts by shifting the desired test data into the boundary-scan register in the Shift-DR controller state. By moving into the Update-DR controller state, data shifting is terminated, and on the falling edge of the TCK, the data from the shift-register stage is transferred onto the parallel output of the latch stage. The external test results are loaded into the shift-register stage from the system input on the next Capture-DR controller state and are examined by shifting the data toward TDO on the next Shift-DR controller state.

During the SAMPLE/PRELOAD instruction, the Shift-DR state is used to shift out the data captured from the system input and output pins for examination during the Capture-DR state. At the same time, the Shift-DR state shifts in test data to be used by the next boundary-scan instruction other than SAMPLE/PRELOAD. The EXTEST instruction is usually initiated following the SAMPLE/PRELOAD instruction. The data preloaded during the SAMPLE/PRELOAD instruction phase becomes available at the parallel output of the boundary-scan cells when the EXTEST becomes the current instruction on the falling edge of TCK in the Update-IR state.

Similarly, the CLAMP instruction is usually initiated following the SAMPLE/PRELOAD instruction. The latched data in the boundary-scan cell becomes available to the system output pins when CLAMP becomes the current instruction and when the bypass register is selected as the data path from TDI to TDO.

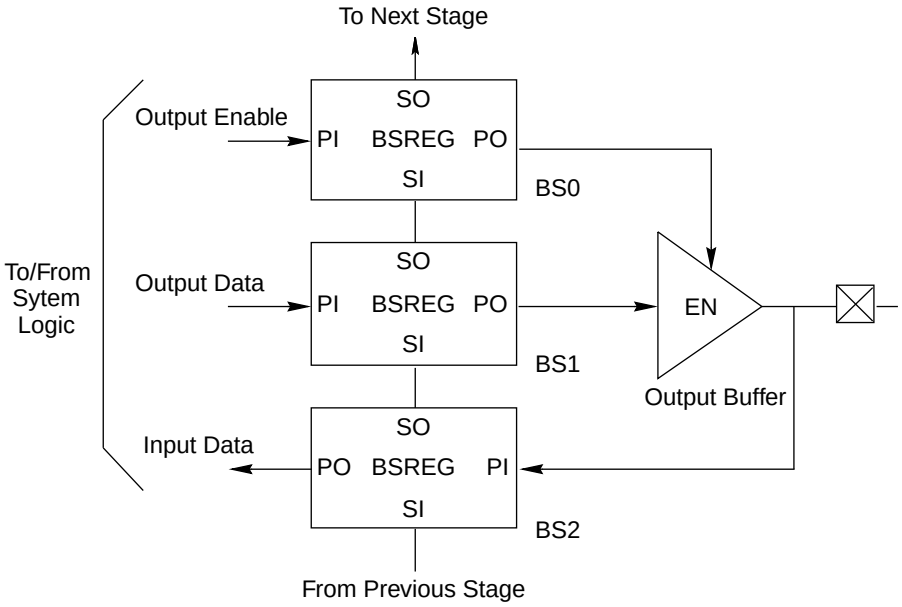


Figure 7 • *Functional Schematic of Boundary-Scan Cell*

Table 5 • *Summary of EXTEST Operation*

Controller State	Boundary-Scan Shift-Register Stage	Boundary-Scan Latch Stage	Parallel Output (PO)
Test-Logic-Reset	Undefined	Undefined	Parallel In = Parallel Out
Capture-DR	Data at PI is loaded	Undefined	Latched Data
Shift-DR	Shift data toward TDO	Undefined	Latched Data
Exit1-DR Exit2-DR Pause-DR	Retain previous state	Undefined	Latched Data
Update-DR	Retain previous state	Latches data from the shift register	Latched Data = Parallel Out (on the falling edge of TCK)
All other states	Retain previous state	Retain previous state	Latched Data

Table 6 • *Summary of SAMPLE/PRELOAD Operation*

Controller State	Boundary-Scan Shift-Register Stage	Boundary-Scan Latch Stage	Parallel Output (PO)
Test-Logic-Reset	Undefined	Undefined	Parallel In = Parallel Out
Capture-DR	Data on PI is loaded	Undefined	Parallel In = Parallel Out
Shift-DR	Shift data toward TDO	Undefined	Parallel In = Parallel Out
Exit1-DR Exit2-DR Pause-DR	Retain previous state	Undefined	Parallel In = Parallel Out
Update-DR	Retain previous state	Latches data from the shift register	Parallel In = Parallel Out
All other states	Retain previous state	Retain previous state	Parallel In = Parallel Out

Note: *During the SAMPLE/PRELOAD instruction, the parallel input and output of the boundary-scan cells are transparent (PI equals PO).*

JPROBE Register

The JPROBE register consists of a 2-bit shift register (labeled "JPRBREG") connected to the existing probe registers, as shown in Figure 8. The registers that are darkened are not parts of the JPROBE register. The presence of the JPROBE register and the JPROBE instruction permits the use of the internal probe circuitry to observe and analyze any signal inside an Actel chip via JTAG.

The desired probe address is shifted into the JPROBE register by first selecting the JPROBE instruction and then moving to the Shift-DR controller state. Shifting is discontinued by entering the Update-DR controller state. The probe results are loaded into the JPRBREG on the rising edge of TCK in the next Capture-DR controller state. The probe results can be examined by moving back to the Shift-DR controller state and shifting the result toward TDO. Table 7 shows the summary of the JPROBE operation. The probe results may also be observed at the probe pins (PRA and PRB), provided that these pins have been reserved for probe use.

During the JPROBE operation, DCLK and SDI inputs are disabled. However, if the current test instruction is different from JPROBE, the probe circuitry can be accessed and operated normally through the probe pins (DCLK, SDI, PRA, and PRB).

Boundary-Scan Description Lanuage (BSDL) File

Conformance to the IEEE Standard 1149.1 requires that the operation of the various JTAG components be documented. The BSDL file provides the standard format to describe the JTAG components which can be used by automatic test equipment software. The file includes the instructions that are supported, instruction bit pattern, and the boundary-scan chain order.

BSDL files for the 3200DX family is available on the Actel World Wide Web Homepage (www.actel.com) and in the Actel ftp site (ftp.actel.com).

Table 7 • *Summary of the Operation of the JPROBE Register*

Controller State	JPRBREG	Probe Register
Test-Logic-Reset	Undefined	Undefined
Capture-DR	Probe result loaded when valid address is in the probe register	Retain previous state
Shift-DR	Shift probe address (probe result) toward TDO	Shift probe address (probe result) toward TDO
Exit1-DR Exit2-DR Pause-DR	Retain previous state	Retain previous state
Update-DR	Retain previous state	Retain previous state
All other states	Undefined	Undefined

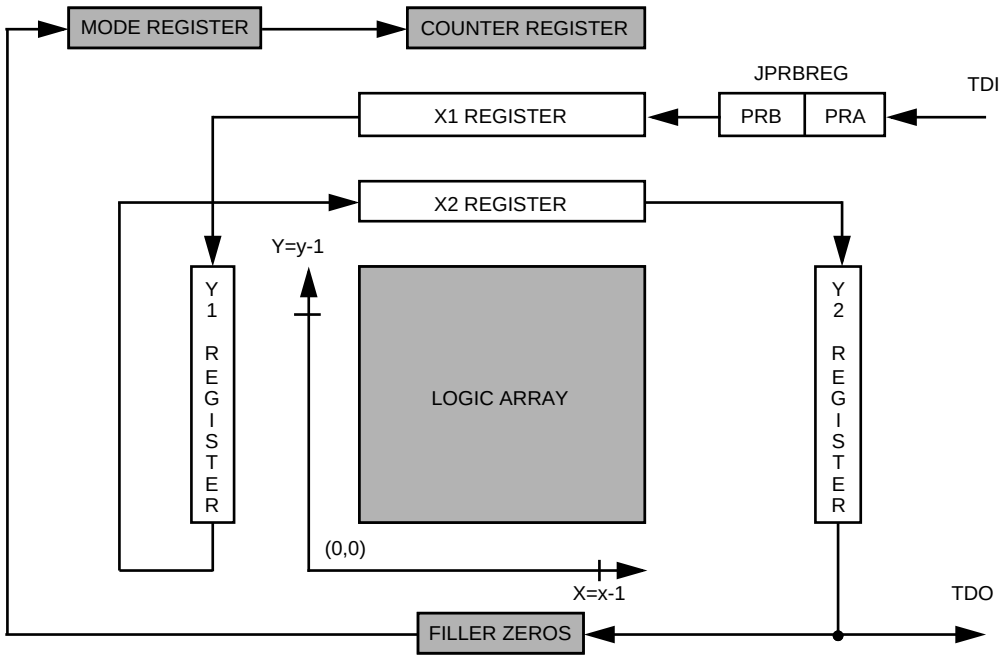


Figure 8 • *Functional Schematic of the JPROBE Register*

References:

1. Colin M. Maunder & Rodham E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. IEEE Computer Society Press, 10662 Los Vaqueros Circle, P.O. Box 3014, Los Alamitos, CA 90720-1264.
2. "IEEE Std 1149.1-1993, IEEE Standard Test Access Port, and Boundary-Scan Architecture." IEEE, Inc., 345 East 47th St., New York, NY 10017-2394.
3. Kenneth P. Parker. *The Boundary-Scan Handbook*. Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, MA 02061.